ICM-45608 Datasheet

High Performance 6-Axis MEMS MotionTracking Device

ICM-45608 HIGHLIGHTS

The ICM-45608 is a high performance 6-axis MEMS MotionTracking device. It has a configurable host interface that supports I3C^{SM}, I^{2}C and SPI serial communication, and an I^{2}C master mode interface for connection to external sensors. The device features up to 8Kbytes FIFO and 2 programmable interrupts.

The ICM-45608 supports the lowest gyro and accel sensor noise in this IMU class, and has the highest stability against temperature, shock (up to 20,000g) or SMT/bend induced offset as well as immunity against out-of-band vibration induced noise. Other industry-leading features include InvenSense on-chip APEX Motion Processing engine for gesture recognition, activity classification, along with programmable digital filters, and an embedded temperature sensor.

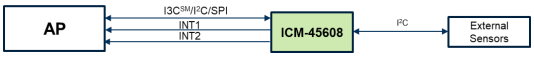
FEATURES

- Gyroscope Noise: 3.8 mdps/√Hz & Accelerometer Noise: 70 µg/√Hz
  - Low-Noise mode 6-axis current consumption of 0.42 mA at 1600Hz
- User selectable Gyro Full-scale range (dps): ±15.625/±31.25/±62.5/±125/±250/±500/±1000/±2000
- User selectable Accelerometer Full-scale range (g): ±2/±4/±8/±16
- User configurable internal pull-up/pull-downs included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs
- User configurable Output Data Rate (ODR) and FIFO Data Rate (FDR)
- User-programmable digital filters for gyro, accel, and temp sensor
- APEX Motion Functions:
  - Single/Double/Triple Tap Detection, Wake on Motion, Free-Fall Detection, Low-G Detection, High-G Detection, 9-Axis Gyro Assisted Fusion, Sensor Inference Framework
- Host interface: 12.9 MHz I3C^{SM}, 1 MHz I^{2}C, 24 MHz SPI

APPLICATIONS

- Game Controllers, Cameras, IoT, Drones, Non-OIS SmartPhones, Wearables, Hearables

BLOCK DIAGRAM



ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-45608†	−40°C to +85°C	2.5x3mm 14-Pin LGA

†Denotes RoHS and Green-Compliant Package

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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-45608 Dual-Interface MotionTracking device. The device is housed in a small 2.5x3x0.81 mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-45608 is a 6-axis MotionTracking device with a configurable host interface that supports I3C^{SM}, I^{2}C and SPI serial communication, and an I^{2}C master mode interface for connection to external sensors. It combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.81 mm (14-pin LGA) package.

ICM-45608 also features up to 8Kbytes FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-45608, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope supports independently programmable full-scale range settings from ±15.625dps to ±2000dps for the UI path, and the accelerometer supports independently programmable full-scale range settings from ±2g to ±16g for the UI path.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I3C^{SM}, I^{2}C and SPI serial interfaces, a VDD operating range of 1.71V to 3.6V, and a separate VDDIO operating range of 1.08V to 3.6V.

The host interface can be configured to support I3C^{SM} slave, I^{2}C slave, or SPI slave modes. The I3C^{SM} interface supports speeds up to 12.9MHz (data rates up to 12.9Mbps in SDR mode, 25.8Mbps in DDR mode), the I^{2}C interface supports speeds up to 1MHz, and the SPI interface supports speeds up to 24MHz.

User configurable internal pull-up/pull-downs are included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, TDK InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.81 mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000*g* shock reliability.

1.3 APPLICATIONS

- Game Controllers
- Cameras
- IoT
- Drones
- Non-OIS SmartPhones
- Wearables
- Hearables

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-45608 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with independently programmable full-scale range of ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000 degrees/sec for UI and auxiliary paths
- Low Noise (LN) and Low Power (LP) power modes support
- Digitally-programmable low-pass filters
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-45608 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with independently programmable full-scale range of ±2*g*, ±4*g*, ±8*g* and ±16*g* for UI and auxiliary paths
- Low Noise (LN) and Low Power (LP) power modes support
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 MOTION FEATURES

ICM-45608 includes the following motion features, also known as APEX:

- Single Tap / Double Tap / Triple Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.
- 9-axis Gyro Assisted Fusion: Handles ICT-1531x magnetometer automatic sampling and provides raw magnetometer data as well as calibrated gyroscope and magnetometer data as well 6-axis and 9-axis fusion data computed from non-calibrated accelerometer and/or calibrated gyroscope data and/or calibrated magnetometer data.
- Sensor Inference Framework: Triggers an interrupt when loaded customer algorithm model has finished classifying an activity and reports the identified activity.

2.4 ADDITIONAL FEATURES

ICM-45608 includes the following additional features:

- Up to 8Kbytes FIFO buffer enables the applications processor to read the data in bursts, default FIFO size is 2Kbytes, user can extend it up to 8kByte by disabling APEX functions
- EDMP Enhanced Digital Motion Processor for implementing motion algorithms
- 20-bits data format support in FIFO for high-data resolution
- User-programmable digital filters for gyroscope, accelerometer, and temperature sensor
- Main interface: 12.5MHz I3C^{SM} (data rates up to 12.5Mbps in SDR mode, 25Mbps in DDR mode) / 1 MHz I^2C / 24 MHz SPI slave host interface
- Auxiliary interface: 400 kHz I^2C master
- User configurable internal pull-up/pull-downs included on I/O interfaces to reduce system costs associated with external pull-ups/pull-downs
- User configurable Output Data Rate (ODR) and FIFO Data Rate (FDR)
- Digital-output temperature sensor
- Smallest and thinnest LGA package for portable devices: 2.5x3x0.81 mm (14-pin LGA)
- 20,000 *g* shock tolerant
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	GYRO_UI_FS_SEL =1		±2000		º/s	3
	GYRO_UI_FS_SEL =2		±1000		º/s	3
	GYRO_UI_FS_SEL =3		±500		º/s	3
	GYRO_UI_FS_SEL =4		±250		º/s	3
	GYRO_UI_FS_SEL =5		±125		º/s	3
	GYRO_UI_FS_SEL =6		±62.5		º/s	3
	GYRO_UI_FS_SEL =7		±31.25		º/s	3
	GYRO_UI_FS_SEL =8		±15.625		º/s	3
Gyroscope ADC Word Length	Output in two's complement format		16		bits	3, 6
Sensitivity Scale Factor	GYRO_UI_FS_SEL =1		16.4		LSB/(º/s)	3
	GYRO_UI_FS_SEL =2		32.8		LSB/(º/s)	3
	GYRO_UI_FS_SEL =3		65.5		LSB/(º/s)	3
	GYRO_UI_FS_SEL =4		131		LSB/(º/s)	3
	GYRO_UI_FS_SEL =5		262		LSB/(º/s)	3
	GYRO_UI_FS_SEL =6		524.3		LSB/(º/s)	3
	GYRO_UI_FS_SEL =7		1048.6		LSB/(º/s)	3
	GYRO_UI_FS_SEL =8		2097.2		LSB/(º/s)	3
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C		±0.5		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C, board-level		±0.01		%/ºC	1, 8
Nonlinearity	Best fit straight line; board-level, 25°C		±0.1		%	1, 8
Cross-Axis Sensitivity	Non-Orthogonality; Board-level		±1		%	1, 8
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	Component-level, 25°C		±0.5		º/s	2
ZRO Change vs. Temperature	-40°C to +85°C, board-level		±0.015		º/s/ºC	1, 8
OTHER PARAMETERS						
Rate Noise Spectral Density	@ 10 Hz, 25°C		0.0038		º/s /√Hz	2, 4
Total RMS Noise	Bandwidth = 100 Hz		0.038		º/s-rms	4, 5
Gyroscope Mechanical Frequencies			29.7		kHz	2
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		35		ms	1, 7
Output Data Rate	Low Noise Mode (LNM)	12.5		6400	Hz	3
	Low Power Mode (LPM)	1.5625		400	Hz	3

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Rate Noise Spectral Density.
6. 20-bits data format supported in FIFO, see section 5.
7. Measurement conditions: Gyroscope ODR = 6400Hz; Register field GYRO_UI_LPFBW_SEL set to 000 (low pass filter bypassed.
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	ACCEL_UI_FS_SEL = 1		±16		*g*	3
	ACCEL_UI_FS_SEL = 2		±8		*g*	3
	ACCEL_UI_FS_SEL = 3		±4		*g*	3
	ACCEL_UI_FS_SEL = 4		±2		*g*	3
ADC Word Length	Output in two's complement format		16		bits	3, 6
Sensitivity Scale Factor	ACCEL_UI_FS_SEL = 1		2,048		LSB/*g*	3
	ACCEL_UI_FS_SEL = 2		4,096		LSB/*g*	3
	ACCEL_UI_FS_SEL = 3		8,192		LSB/*g*	3
	ACCEL_UI_FS_SEL = 4		16,384		LSB/*g*	3
Sensitivity Scale Factor Initial Tolerance	Component-level, 25°C		±0.5		%	2
Sensitivity Change vs. Temperature	-40°C to +85°C, board-level		±0.01		%/ºC	1, 8
Nonlinearity	Best fit straight line, ±2g; board-level, 25°C		±0.1		%	1, 8
Cross-Axis Sensitivity	Non-Orthogonality; Board-level		±1		%	1, 8
ZERO-G OUTPUT						
Initial Tolerance	Component-level, 25°C		±15		m*g*	2
Zero-G Level Change vs. Temperature	-40°C to +85°C, board-level		±0.2		m*g*/ºC	1, 8
OTHER PARAMETERS						
Noise Spectral Density	@ 10 Hz; Up to ±8g FSR		70		µ*g*/√Hz	2, 4
	@ 10 Hz; ±16g FSR		80		µ*g*/√Hz	2, 4
RMS Noise	Bandwidth = 100 Hz; Up to ±8g FSR		0.7		mg-rms	4, 5
	Bandwidth = 100 Hz; ±16g FSR		0.8		mg-rms	4, 5
Accelerometer Startup Time	From sleep mode to valid data		10		ms	1, 7
Output Data Rate	Low Noise Mode (LNM)	12.5		6400	Hz	3
	Low Power Mode (LPM)	1.5625		400	Hz	3

Table 2. Accelerometer Specifications

Notes:

1. Derived from validation or characterization of parts, not tested in production.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.
5. Calculated from Rate Noise Spectral Density.
6. 20-bits data format supported in FIFO, see section 5.
7. Measurement conditions: Gyroscope ODR = 6400Hz; Register field GYRO_UI_LPFBW_SEL set to 000 (low pass filter bypassed.
8. Board-level specs performance depends on specific board design of TDK-InvenSense test boards and may not be directly reproducible with other board designs.

3.3 ELECTRICAL SPECIFICATIONS

3.3.1 D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.6	V	1
VDDIO		1.08*	1.8	3.6	V	1
SUPPLY CURRENTS						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer (1600Hz ODR)		420		µA	2
	6-Axis Gyroscope + Accelerometer (6400Hz ODR)		440		µA	2
	3-Axis Accelerometer (1600Hz ODR)		125		µA	2
	3-Axis Accelerometer (6400Hz ODR)		130		µA	2
	3-Axis Gyroscope (1600Hz ODR)		365		µA	2
	3-Axis Gyroscope (6400Hz ODR)		375		µA	2
Low-Power Mode	6-Axis Gyroscope + Accelerometer (50Hz ODR; Gyro 10x AVG; Accel 4x AVG)		220		µA	2
	3-Axis Accelerometer (50Hz ODR; 4x AVG)		67		µA	2
	3-Axis Gyroscope (50Hz ODR; 10x AVG)		210		µA	2
Ultra Low-Power Mode	3-Axis Accelerometer (50Hz ODR; 1x AVG)		15		µA	2
Full-Chip Sleep Mode	At 25ºC		2.2		µA	2
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		+85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Guaranteed by design.
2. Derived from validation or characterization of parts, not tested in production.

* Important Note: When using I3C^{SM} interface the minimum VDDIO value is 1.1V.

3.3.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Valid power-on RESET Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		1	ms	1
Power Supply Noise	V_{DD}=1.8V or 3.6V, up to 1MHz		10	50	mV peak-peak	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output	Output in two's complement format		0		LSB	3
ADC Resolution			16		bits	2
ODR	With Filter	1.5625		3200	Hz	2, 4
Room Temperature Offset	25°C	-5		5	°C	3
Stabilization Time (fixed number of clock cycles)				0.014	sec	2
Sensitivity	Trimmed		128		LSB/°C	1
Sensitivity for FIFO data	Trimmed		2		LSB/°C	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			1	ms	1
I²C ADDRESS						
I²C ADDRESS	AP_AD0 = 0 AP_AD0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SCLK, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	1
V_{IL}, Low Level Input Voltage		-0.5V		0.3*VDDIO	V	
C_I, Input Capacitance			<10		pF	
DIGITAL OUTPUT (SDO, INT1, INT2)						
V_{OH}, High Level Output Voltage	R_{LOAD}=1 MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD}=1 MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t_{INT}, INT Pulse Width	int0_tpulse_duration= 0 , 1 (100µs, 8µs) int1_tpulse_duration= 0 , 1 (100µs, 8µs)		100 or 8	100	µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW-Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL}=0.4 V V_{OL}=0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Clock Frequency Initial Tolerance	Gyro inactive; 25°C	-1.25		+1.25	%	1
	Gyro active; 25°C	-1.25		+1.25	%	1
Frequency Variation over Temperature	Gyro inactive; -40°C to +85°C			±3	%	1
	Gyro active; -40ºC to +85ºC			±1	%	1

Table 4. D.C. Electrical Characteristics

Notes:

1. Based on design. Not tested in production.
2. Guaranteed by design.
3. Production tested.
4. Temperature sensor ODR is the higher value between gyroscope and accelerometer ODR.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING (Host Interface)	**I²C FAST-MODE PLUS**					
f_{SCL}, SCL Clock Frequency				1	MHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.26			µs	1
t_{LOW}, SCL Low Period		0.50			µs	1
t_{HIGH}, SCL High Period		0.26			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.26			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		50			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 30 to 130 pF			120	ns	1, 2
t_f, SDA and SCL Fall Time	C_b bus cap. from 30 to 130 pF	20 x (VDD / 5.5 V)		120	ns	1, 2
$t_{SU.STO}$, STOP Condition Setup Time		0.26			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		0.50			µs	1
C_b, Capacitive Load for each Bus Line		30		130	pF	1
$t_{VD.DAT}$, Data Valid Time				0.45	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.45	µs	1

Table 5. I²C Host Interface Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Transition times are defined between thresholds: 0.3*VDDIO, 0.7*VDDIO.

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
I²C TIMING (Master Interface)	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.60			µs	1
t_{LOW}, SCL Low Period		1.30			µs	1
t_{HIGH}, SCL High Period		0.60			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.60			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 30 to 200 pF	20		300	ns	1, 2
t_f, SDA and SCL Fall Time	C_b bus cap. from 30 to 200 pF	20 x (VDD / 5.5 V)		300	ns	1, 2
$t_{SU.STO}$, STOP Condition Setup Time				0.60	µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.30			µs	1
C_b, Capacitive Load for each Bus Line		30		200	pF	1
$t_{VD.DAT}$, Data Valid Time				0.90	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.90	µs	1

Table 6. I²C Master Interface Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.
2. Transition times are defined between thresholds: 0.3*VDDIO, 0.7*VDDIO.

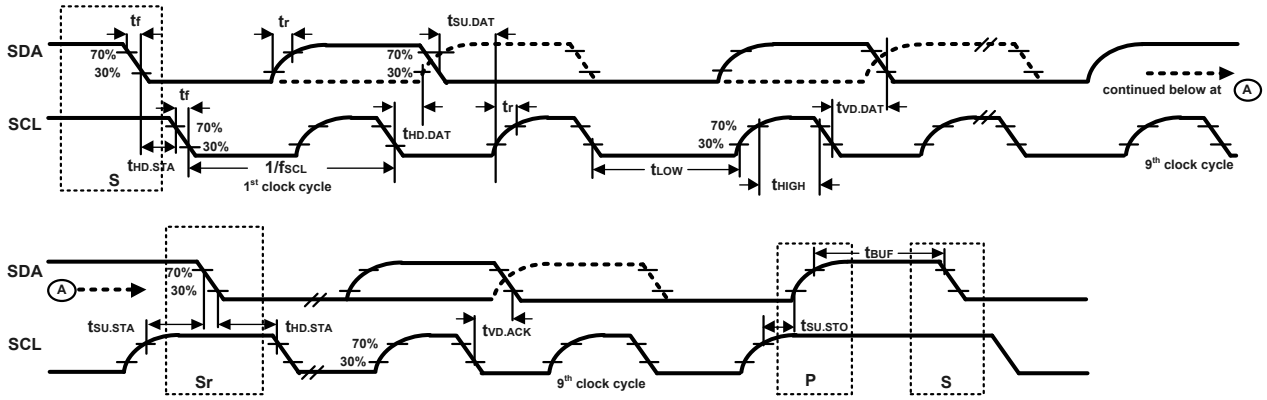

Figure 1. I²C Bus Timing Diagram

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3.5 SPI TIMING CHARACTERIZATION – 4-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	VDDIO < 1.71V		VDDIO ≥ 1.71V			
		MIN	MAX	MIN	MAX	UNITS	NOTES
SPI TIMING							
f_{SPC}, SCLK Clock Frequency	Default		20		24	MHz	1
t_{LOW}, SCLK Low Period		23.5		17		ns	1
t_{HIGH}, SCLK High Period		22.5		17		ns	1
$t_{SU.CS}$, CS Setup Time		17		17		ns	1
$t_{HD.CS}$, CS Hold Time		5		5		ns	1
$t_{SU.SDI}$, SDI Setup Time		13		13		ns	1
$t_{HD.SDI}$, SDI Hold Time		8		8		ns	1
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20 pF		18.5		18.5	ns	1
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20 pF	3.5		3.5		ns	1
$t_{DIS.SDO}$, SDO Output Disable Time			28		28	ns	1

Table 7. 4-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

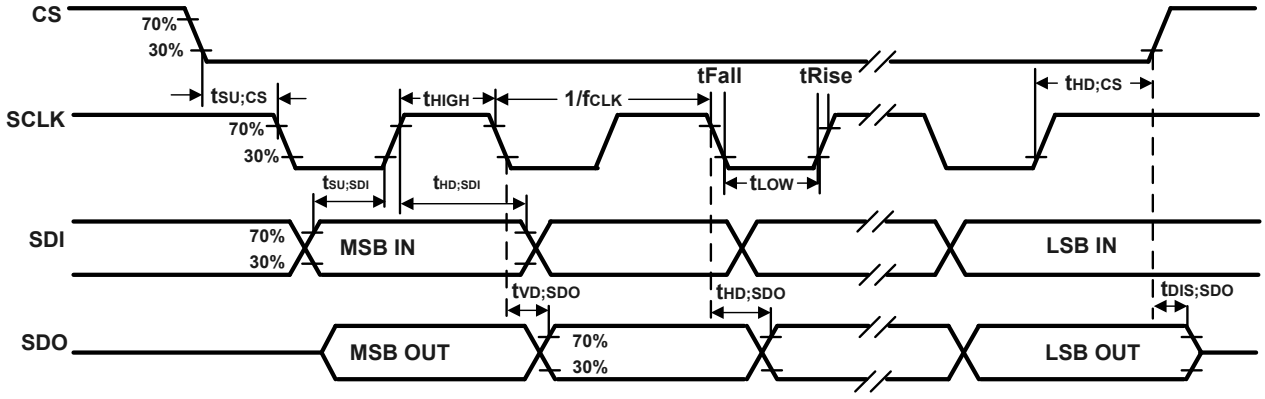

Figure 2. 4-Wire SPI Bus Timing Diagram

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3.6 SPI TIMING CHARACTERIZATION – 3-WIRE SPI MODE

Typical Operating Circuit of section 4.2, VDD = 1.8 V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	VDDIO < 1.71V		VDDIO ≥ 1.71V			
		MIN	MAX	MIN	MAX	UNITS	NOTES
SPI TIMING							
f_{SPC}, SCLK Clock Frequency	Default		20		24	MHz	1
t_{LOW}, SCLK Low Period		23.5		17		ns	1
t_{HIGH}, SCLK High Period		22.5		17		ns	1
$t_{SU.CS}$, CS Setup Time		17		17		ns	1
$t_{HD.CS}$, CS Hold Time		5		5		ns	1
$t_{SU.SDIO}$, SDIO Input Setup Time		13		13		ns	1
$t_{HD.SDIO}$, SDIO Input Hold Time		8		8		ns	1
$t_{VD.SDIO}$, SDIO Output Valid Time	C_{load} = 20 pF		18.5		18.5	ns	1
$t_{HD.SDIO}$, SDIO Output Hold Time	C_{load} = 20 pF	3.5		3.5		ns	1
$t_{DIS.SDIO}$, SDIO Output Disable Time			28		28	ns	1

Table 8. 3-Wire SPI Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

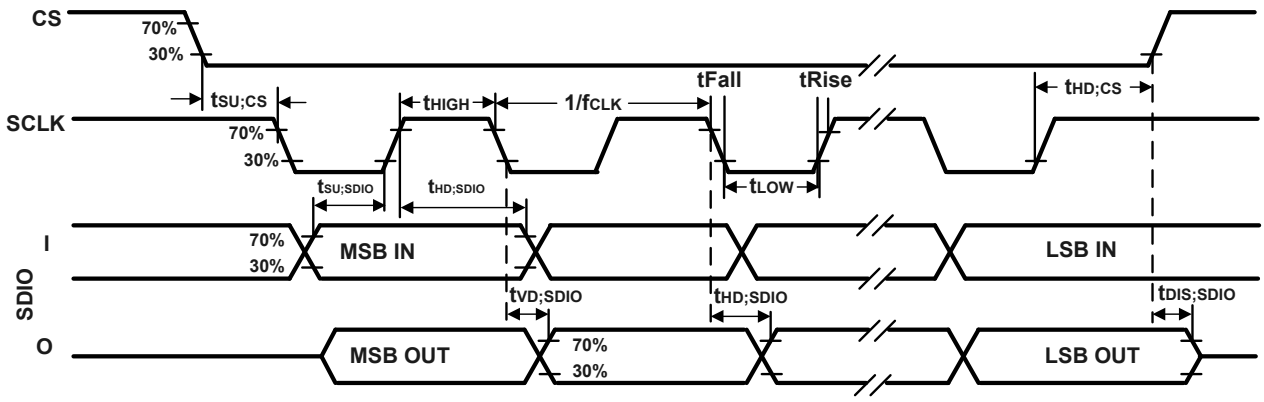

Figure 3. 3-Wire SPI Bus Timing Diagram

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3.7 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
Input Voltage Level (FSYNC, SCL, SDA)	-0.5 V to VDDIO + 0.5 V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 500 V (CDM)
Latch-up	JEDEC Class II (2), 125°C ±100 mA

Table 9. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Single Interface Mode	Dual Interface I²C Master Mode	Notes
1	AP_SDO / AP_AD0	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I²C slave address LSB	AP_SDO: AP SPI serial data output (4-wire mode); AP_AD0: AP I3C^{SM} / I²C slave address LSB	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sdo_pe_trim_d2a[0] and pads_ap_sdo_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_ap_sdo_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sdo_pud_trim_d2a[0] = 0 (1). If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sdo_pe_trim_d2a[0] = 0.
2	RESV / MAS_DA	RESV: No Connect or Connect to VDDIO or Connect to GND	MAS_DA: I²C serial master data	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_sdi_pe_trim_d2a[0] and pads_aux1_sdi_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_sdi_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sdi_pud_trim_d2a[0] = 0 (1). If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sdi_pe_trim_d2a[0] = 0. If pin2 is no connect, leave pads_aux1_sdi_pe_trim_d2a[0] = 1. If pin2 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sdi_pe_trim_d2a[0] = 0.
3	RESV / MAS_CLK	RESV: No Connect or Connect to VDDIO or Connect to GND	MAS_CLK: I²C serial master clock	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_sclk_pe_trim_d2a[0] and pads_aux1_sclk_pud_trim_d2a[0] Internal pull-up can be disabled (enabled) by configuring pads_aux1_sclk_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sclk_pud_trim_d2a[0] = 0 (1). If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sclk_pe_trim_d2a[0] = 0. If pin3 is no connect, leave pads_aux1_sclk_pe_trim_d2a[0] = 1. If pin3 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sclk_pe_trim_d2a[0] = 0.
4	INT1 / INT	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All	INT1: Interrupt 1 (Note: INT1 can be push-pull or open drain); INT: All interrupts mapped to pin 4	By default, internal pull-up is disabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal

		interrupts mapped to pin 4		pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_int1_pe_trim_d2a[0] and pads_int1_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_int1_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_int1_pud_trim_d2a[0] = 0 (1).
5	VDDIO	VDDIO: IO power supply voltage	VDDIO: IO power supply voltage	
6	GND	GND: Power supply ground	GND: Power supply ground	
7	RESV	RESV: No Connect or Connect to VDDIO or Connect to GND	RESV: No Connect or Connect to VDDIO or Connect to GND	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_pin7_pe_trim_d2a[0] and pads_pin7_cs_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_pin7_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_pin7_cs_pud_trim_d2a[0] = 0 (1). If pin7 is no connect, leave pads_pin7_pe_trim_d2a[0] = 1. If pin7 is connected to VDDIO or GND, disable internal pull-up by setting pads_pin7_pe_trim_d2a[0] = 0.
8	VDD	VDD: Power supply voltage	VDD: Power supply voltage	
9	INT2 / FSYNC	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; If pin not used, can be No Connect or Connect to VDDIO	INT2: Interrupt 2 (Note: INT2 can be push-pull or open drain); FSYNC: Frame sync input; If pin not used, can be No Connect or Connect to VDDIO	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_int2_pe_trim_d2a[0] and pads_int2_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_int2_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_int2_pud_trim_d2a[0] = 0 (1). If pin9 is no connect, leave pads_int2_pe_trim_d2a[0] = 1. If pin9 is connected as an I/O, disable internal pull-up by setting pads_int2_pe_trim_d2a[0] = 0.
10	RESV	RESV: No Connect or Connect to VDDIO or Connect to GND	RESV: No Connect or Connect to VDDIO or Connect to GND	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_aux1_cs_pe_trim_d2a[0] and pads_aux1_cs_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_cs_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_cs_pud_trim_d2a[0] = 0 (1). If the AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_cs_pe_trim_d2a[0] = 0. If pin10 is no connect, leave pads_aux1_cs_pe_trim_d2a[0] = 1. If pin10 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_cs_pe_trim_d2a[0] = 0.
11	RESV	RESV: No Connect or Connect to VDDIO or Connect to GND	RESV: No Connect or Connect to VDDIO or Connect to GND	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers

				pads_aux1_sdo_pe_trim_d2a[0] and pads_aux1_sdo_pud_trim_d2a[0]. Internal pull-up can be disabled (enabled) by configuring pads_aux1_sdo_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_aux1_sdo_pud_trim_d2a[0] = 0 (1). If AUX1 interface is active, the internal pull-up should be disabled by setting pads_aux1_sdo_pe_trim_d2a[0] = 0. If pin11 is no connect, leave pads_aux1_sdo_pe_trim_d2a[0] = 1. If pin11 is connected to VDDIO or GND, disable internal pull-up by setting pads_aux1_sdo_pe_trim_d2a[0] = 0.
12	AP_CS	AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface	AP_CS: AP SPI Chip select (AP SPI interface); Connect to VDDIO if using AP I3C^{SM} / I^{2}C interface	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_cs_pe_trim_d2a[0] and pads_ap_cs_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_cs_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_cs_pud_trim_d2a[0] = 0 (1). If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_cs_pe_trim_d2a[0] = 0.
13	AP_SCL / AP_SCLK	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock	AP_SCL: AP I3C^{SM} / I^{2}C serial clock; AP_SCLK: AP SPI serial clock	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sclk_pe_trim_d2a[0] and pads_ap_sclk_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_sclk_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sclk_pud_trim_d2a[0] = 0 (1). If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sclk_pe_trim_d2a[0] = 0.
14	AP_SDA / AP_SDIO / AP_SDI	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)	AP_SDA: AP I3C^{SM} / I^{2}C serial data; AP_SDIO: AP SPI serial data I/O (3-wire mode); AP_SDI: AP SPI serial data input (4-wire mode)	By default, internal pull-up is enabled. The internal weak pull-up is not strong enough to replace a pull-up resistor usually used on an open-drain bus. This pin supports both internal pull up and pull-down functionality. Internal pull up/down is controlled by two registers pads_ap_sdi_pe_trim_d2a[0] and pads_ap_sdi_pud_trim_d2a[0]. Internal pull can be disabled (enabled) by configuring pads_ap_sdi_pe_trim_d2a[0] = 0 (1) and internal pull direction down (up) can be set by pads_ap_sdi_pud_trim_d2a[0] = 0 (1). If the AP interface is active, the internal pull-up should be disabled by setting pads_ap_sdi_pe_trim_d2a[0] = 0.

Table 10. Signal Descriptions

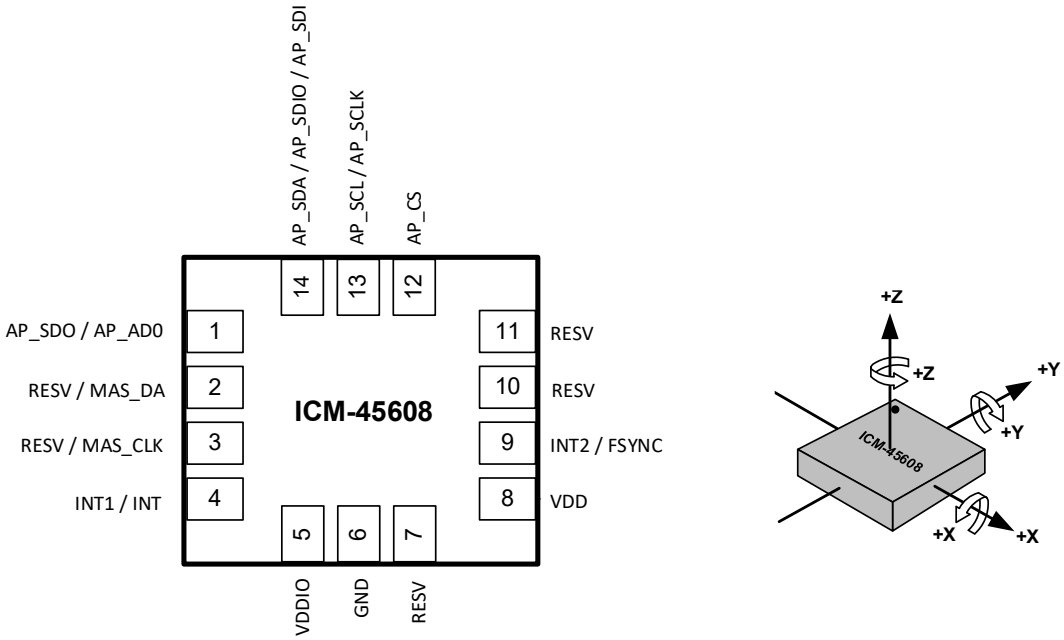

Figure 4. Pin Out Diagram for ICM-45608 2.5x3.0x0.81 mm LGA

4.2 TYPICAL OPERATING CIRCUIT (DUAL INTERFACE I²C MASTER MODE)

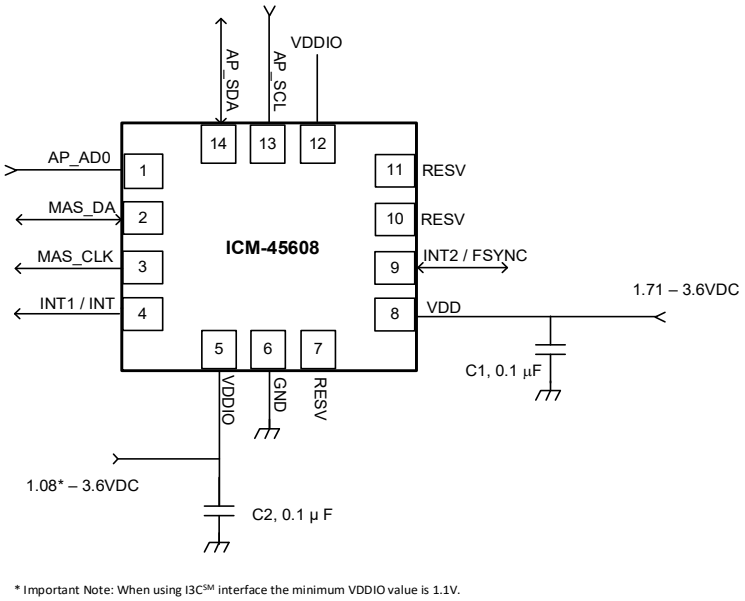

Figure 5. ICM-45608 Application Schematic Dual Interface I²C Master Mode (I3C℠ / I²C Interface to Host)

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

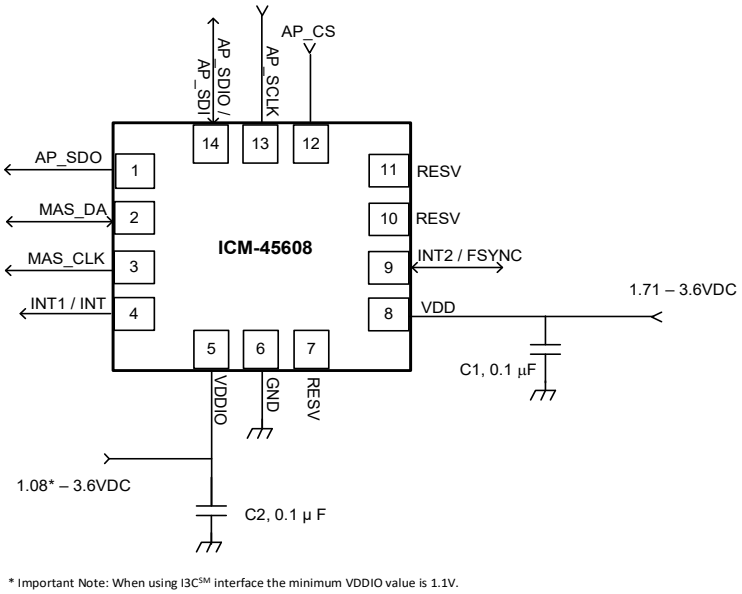

Figure 6. ICM-45608 Application Schematic Dual Interface I²C Master Mode (SPI Interface to Host)

4.3 TYPICAL OPERATING CIRCUIT (SINGLE INTERFACE MODE)

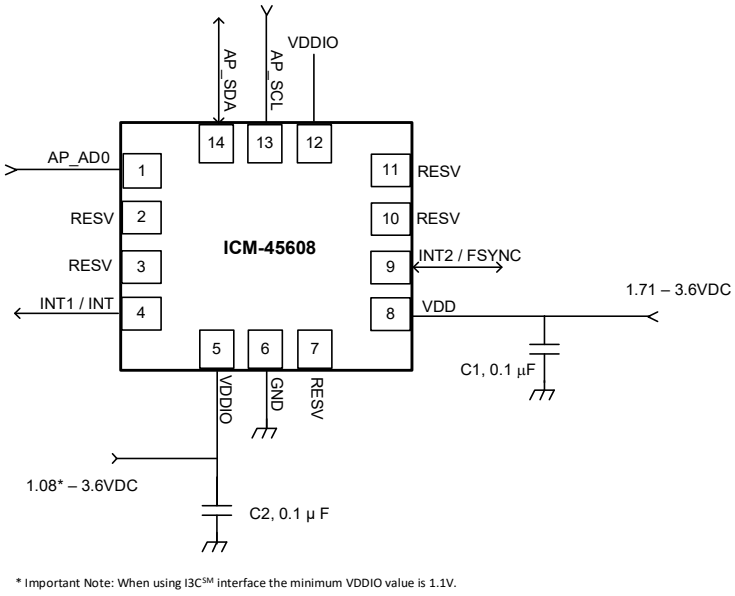

Figure 7. ICM-45608 Application Schematic Single Interface Mode (I3C^SM / I²C Interface to Host)

Note: I²C lines are open drain and pull-up resistors (e.g. 10 kΩ) are required.

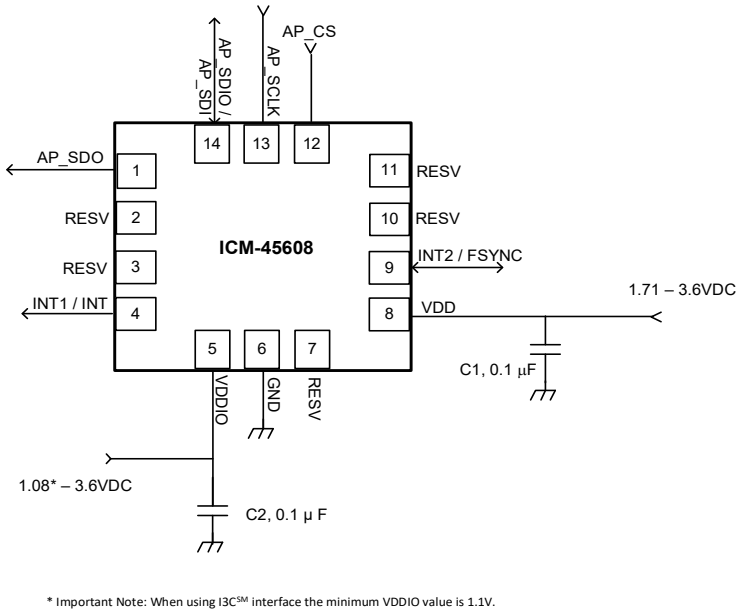

Figure 8. ICM-45608 Application Schematic Single Interface Mode (SPI Interface to Host)

4.4 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
VDD Bypass Capacitor	C1	X7R, 0.1µF ±10%	1
VDDIO Bypass Capacitor	C2	X7R, 0.1µF ±10%	1

Table 11. Bill of Materials

Note: Use larger bypass capacitor than 0.1µF if power supply ripple exceeds 50mV peak-to-peak.

4.5 SYSTEM BLOCK DIAGRAM

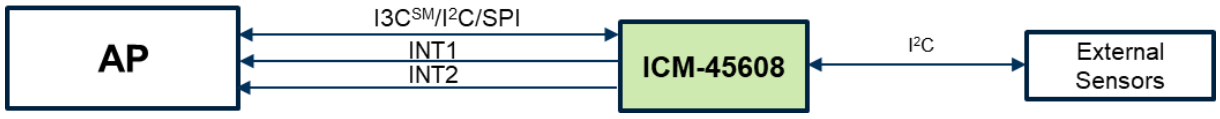

Figure 9. ICM-45608 System Block Diagram

Note: The above block diagram is an example. Please refer to the pin-out (section 4.1) for other configuration options.

4.6 OVERVIEW

The ICM-45608 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
  - 20-bits data format support in FIFO for high-data resolution (see section 5 for details)
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
  - 20-bits data format support in FIFO for high-data resolution (see section 5 for details)
- I3C^{SM}, I^{2}C and SPI Host Interface
- I^{2}C Master Interface for connection to external sensors
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.7 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-45608 includes a vibratory MEMS rate gyroscope, which detects rotation about the X-, Y-, and Z- Axes. When the gyroscope is rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using on-chip Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±15.625, ±31.25, ±62.5, ±125, ±250, ±500, ±1000, and ±2000degrees per second (dps).

4.8 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-45608 includes a 3-Axis MEMS accelerometer. Acceleration along a particular axis induces displacement of a proof mass in the MEMS structure, and capacitive sensors detect the displacement. The ICM-45608 architecture reduces the accelerometers' susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0*g* on the X- and Y-axes and +1*g* on the Z-axis. The accelerometers' scale factor is calibrated at the factory and is nominally independent of supply voltage. The full-scale range of the digital output can be adjusted to ±2*g*, ±4*g*, ±8*g,* and ±16*g*.

4.9 I3C^{SM}, I^{2}C AND SPI HOST INTERFACE

The ICM-45608 communicates to the application processor using an I3C^{SM}, I^{2}C, or SPI serial interface. The ICM-45608 always acts as a slave when communicating to the application processor.

4.10 I^{2}C MASTER INTERFACE FOR CONNECTION TO EXTERNAL SENSORS

The ICM-45608 has an I^{2}C master interface for connection to external sensors.

Up to 2 external sensors can be connected on this interface and their data read into the ICM-45608. I^{2}C speed up to 400kHz is supported on the master interface. After I^{2}C master finishes reading sensor data from the external sensor(s), the received sensor data is then reformatted by the internal processor (eDMP). The reformatted external sensor data is then moved into FIFO along with other internal sensor data. The external host reads the FIFO to retrieve both the external sensor data and the internal sensor data.

- Independent of the number of external devices on the I^{2}C bus, the I^{2}C master automatically executes up to 4 I^{2}C transactions per trigger.
- The 4 I^{2}C transactions are fully independent to each other.
- Each I^{2}C transaction can be targeting any external I^{2}C device (capped at 2 external I^{2}C devices).
- Each I^{2}C transaction can be a read or a write access transaction.
- Each I^{2}C transaction can be a burst or a non-burst access transaction.
- A read transaction can be from an auto-incremented address location, or from a new address location.
- A read operation with a new address location consumes one of the 4 I^{2}C transactions per trigger.

4.11 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.12 CLOCKING

The ICM-45608 has a flexible clocking scheme, allowing internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

For internal sources, the only setting supporting specified performance in all modes is option b). It is recommended that option b) be used when using internal clock source.

4.13 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers and are accessed via the serial interface. Data from these registers may be read anytime.

4.14 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the interrupt pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO watermark; (5) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.15 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-45608 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

Temperature sensor register data TEMP_DATA is updated with new data at max (Accelerometer ODR, Gyroscope ODR).

4.16 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-45608.

4.17 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.18 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-45608.

Name	Gyro	Accel
Sleep Mode	Off	Off
Standby Mode	Drive On	Off
Accelerometer Low-Power Mode	Off	Duty-Cycled
Accelerometer Ultra Low-Power Mode	Off	Duty-Cycled
Gyroscope Low-Power Mode	Duty-Cycled	Off
6-Axis Low-Power Mode	Duty-Cycled	Duty-Cycled
Accelerometer Low-Noise Mode	Off	On
Gyroscope Low-Noise Mode	On	Off
6-Axis Low-Noise Mode	On	On

Table 12. Standard Power Modes for ICM-45608

5 FIFO

The ICM-45608 contains up to 8Kbytes FIFO (default FIFO size is 2Kbytes, user can extend it up to 8Kbytes by disabling APEX functions) that is accessible via the serial interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyroscope data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO.

ICM-45608 includes FIFO Compression algorithm that allows storing compressed sensor data in FIFO frames, thus virtually providing more FIFO space. It allows to store up to 4 times the number of frames with respect to non-compressed data. Frame decompression must be performed on the Host which reads the FIFO. Compression algorithm uses a hardware lossless algorithm, based on data variation analysis of each axis. Compression ratios x2, x3, x4 are supported, providing up to 32kByte data storage capability.

A 20-bit data format support is included in one of the FIFO packets structures. When the 20-bit data format is used, the gyroscope data consists of 20-bit of actual data, the accelerometer data consists of 19-bit of actual data and the LSB is always set to 0. Irrespective of the user-full scale selection, this high-resolution 20-bit data format is always scaled to ±4000dps (131.1 LSB/dps) for gyroscope and ±32g (16384 LSB/g) for accelerometer.

FIFO packet decimation capability is provided for additional storage optimization. User can configure the FIFO Data Rate (FDR) to control the decimation rate for writing packets to the FIFO. User must disable sensors when initializing FDR control value or making changes to it.

5.1 PACKET STRUCTURE

FIFO packets are assembled in different packet sizes based on the enabled sensors. When internal sensors Accel and Gyro are enabled, the following packets are available:

- 8 bytes packet: Contains Accel-only or Gyro-only data and Temperature data (1 byte)
- 16 bytes packet: Contains Accel data, Gyro data, Temperature data (1 byte), Timestamp
- 20 bytes packet: Contains high-resolution Accel data, Gyro data, Temperature data (2 bytes), Timestamp

The following figure shows packets organization for each format (big endian mode).

Accel-only (8 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Temp (1 byte)	

Gyro-only (8 bytes)

	7	0
0	Header	
1	Gx H	
2	Gx L	
3	Gy H	
4	Gy L	
5	Gz H	
6	Gz L	
7	Temp (1 byte)	

Accel+Gyro (16 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Gx H	
8	Gx L	
9	Gy H	
10	Gy L	
11	Gz H	
12	Gz L	
13	Temp (1 byte)	
14	Timestamp H	
15	Timestamp L	

Accel+Gyro High Resolution (20 bytes)

	7	0
0	Header	
1	Ax H	
2	Ax L	
3	Ay H	
4	Ay L	
5	Az H	
6	Az L	
7	Gx H	
8	Gx L	
9	Gy H	
10	Gy L	
11	Gz H	
12	Gz L	
13	Temp H	
14	Temp L	
15	Timestamp H	
16	Timestamp L	
17	Ax LSB	Gx LSB
18	Ay LSB	Gy LSB
19	Az LSB	Gz LSB

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When external sensors ES0 and ES1 are enabled, the following packets are available:

- 16 bytes packet: Contains 6/9 bytes ES0-only or ES1-only data
- 20 bytes frame: Contains 6/9 bytes ES0 data and ES1 data
- 32 bytes frame: Contains Accel data, Gyro data, 6/9 bytes ES0 data, ES1 data, Temperature data (1 byte), Timestamp. The 32 bytes format is always selected when at least one internal sensor and one external sensor are enabled

The following figure shows packets organization for each format (big endian mode).

5.2 FIFO HEADER

The following table shows the structure of the first byte of the FIFO header.

Bit Field	Item	Description
7	EXT_HEADER	1: FIFO header length is extended to 2 bytes. The second byte is used for compressed frame decoding fields or external sensors information 0: FIFO header length is 1 byte
6	ACCEL_EN	1: Accel is enabled or high resolution is enabled 0: Accel is not enabled and high resolution is not enabled
5	GYRO_EN	1: Gyro is enabled or high resolution is enabled 0: Gyro is not enabled and high resolution is not enabled
4	HIRES_EN	1: High-resolution is enabled (20-bytes format) 0: High-resolution is not enabled
3	TMST_FIELD_EN	1: Timestamp field is included in the packet. This requires that: a) high-resolution is enabled, or b) both Accel and Gyro are enabled, or c) either Accel or Gyro are enabled, and either ES0 or ES1 are enabled The timestamp field contains the timestamp value or FSYNC-ODR delay depending on configuration 0: Timestamp field is not included in the packet
2	FSYNC_TAG_EN	1: FSYNC is triggered and the Timestamp field contains the FSYNC-ODR delay 0: FSYNC is not triggered and the Timestamp field does not contain the FSYNC-ODR delay

1	ACCEL_ODR	1: The ODR for accel is different for this accel data packet compared to the previous accel packet 0: The ODR for accel is the same as the previous packet with accel
0	GYRO_ODR	1: The ODR for gyro is different for this gyro data packet compared to the previous gyro packet 0: The ODR for gyro is the same as the previous packet with gyro

When External Sensors are enabled, an additional header byte is used. The second byte of the header is described below.

Bit Field	Item	Description
7:5	-	Reserved
4	ES0_6b_9b	Indicates how many bytes sensor ES0 provides 1: Sensor ES0 provides 9 bytes data 0: Sensor ES0 provides 6 bytes data
3	ES1_VLD	1: ES1 data is valid 0: ES1 data is not valid
2	ES0_VLD	1: ES0 data is valid 0: ES0 data is not valid
1	ES1_EN	1: Sensor ES1 is enabled 0: Sensor ES1 is not enabled
0	ES0_EN	1: Sensor ES0 is enabled 0: Sensor ES0 is not enabled

6 PROGRAMMABLE INTERRUPTS

The ICM-45608 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. There are two interrupt outputs. Any interrupt may be mapped to either interrupt pin as explained in the register section. The following configuration options are available for the interrupts:

- INT1 and INT2 can be push-pull or open drain
- Level or pulse mode
- Active high or active low

Additionally, ICM-45608 includes In-band Interrupt (IBI) support for the I3C^{SM} interface.

7 EDMP

The on-chip Enhanced Digital Motion Processor (EDMP) is designed for motion processing of next-gen sensor products. It enables ultra-low power run-time and offloads computation of motion processing and sensor fusion algorithms from the host processor. It enables the host system to execute custom algorithms and issue software interrupts to the external environment. The EDMP can be deployed in the system to minimize system level power, simplify the software architecture, and save valuable MIPS on the host processor. The EDMP implements a motion sensor optimized custom ISA with special motion processing instructions.

8 APEX MOTION FUNCTIONS

The APEX features of ICM-45608 consist of:

- Single Tap / Double Tap / Triple Tap Detection: Issues an interrupt when a tap is detected, along with the tap type.
- Wake on Motion: Detects motion when accelerometer data exceeds a programmable threshold.
- Freefall Detection: Triggers an interrupt when device freefall is detected and outputs freefall duration.
- Low-G Detection: Triggers an interrupt when absolute value of accelerometer combined axis falls below a programmable threshold and stays below the threshold for a programmable time.
- High-G Detection: Triggers an interrupt when absolute value of accelerometer goes above a programmable threshold and stays above the threshold for a programmable time.
- 9-axis Gyro Assisted Fusion: Handles ICT-1531x magnetometer automatic sampling and provides raw magnetometer data as well as calibrated gyroscope and magnetometer data as well 6-axis and 9-axis fusion data computed from non-calibrated accelerometer and/or calibrated gyroscope data and/or calibrated magnetometer data.
- Sensor Inference Framework: Triggers an interrupt when loaded customer algorithm model has finished classifying an activity and reports the identified activity.

These functions are run as software on EDMP.

9 DIGITAL INTERFACE

9.1 I3C^{SM}, I^{2}C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-45608 can be accessed using I3C^{SM} at 12.5 MHz (data rates up to 12.5 Mbps in SDR mode, 25 Mbps in DDR mode), I^{2}C at 1 MHz or SPI at 24 MHz. SPI operates in 3-wire or 4-wire mode. Pin assignments for serial interfaces are described in section 4.

9.2 I3C^{SM} INTERFACE

I3C^{SM} is a new 2-wire digital interface comprised of the signals serial data (SDA) and serial clock (SCLK). I3C^{SM} is intended to improve upon the I^{2}C interface, while preserving backward compatibility. The I3C^{SM} capability of this device is compliant with Version 1.1.1 of the MIPI Alliance Specification for I3C^{SM}. Please refer to the corresponding MIPI I3C^{SM} specification for I3C^{SM} timing information for this device.

I3C^{SM} carries the advantages of I^{2}C in simplicity, low pin count, easy board design, and multi-drop (vs. point to point), but provides the higher data rates, simpler pads, and lower power of SPI. I3C^{SM} adds higher throughput for a given frequency, in-band interrupts (from slave to master), dynamic addressing.

ICM-45608 supports the following features of I3C^{SM}:

- SDR data rate up to 12.5 Mbps
- DDR data rate up to 25 Mbps
- Dynamic address allocation
- In-band Interrupt (IBI) support
- Support for asynchronous timing control mode 0
- Error detection (CRC and/or Parity)
- Common Command Code (CCC)

The ICM-45608 always operates as an I3C^{SM} slave device when communicating to the system processor, which thus acts as the I3C^{SM} master. I3C^{SM} master controls an active pullup resistance on SDA, which it can enable and disable. The pullup resistance may be a board level resistor controlled by a pin, or it may be internal to the I3C^{SM} master.

The following table shows I3C^{SM} Common Command Code (CCC) commands supported by the device.

CCC Description			Required or Optional per I3C v1.0	Supported by ICM-45608 Host Interface
	1	ENEC, broadcast mode. (Enable Events).	Required	Yes
	2	DISEC, broadcast mode. (Disable Events)	Required	Yes
	3	ENTAS0, broadcast mode. (Enter Activity State 0)	Required	Yes
	4	ENTAS1, broadcast mode. (Enter Activity State 1)	Optional	No
	5	ENTAS2, broadcast mode. (Enter Activity State 0)	Optional	No
	6	ENTAS3, broadcast mode. (Enter Activity State 0)	Optional	No
	7	RSTDAA, broadcast mode. (Reset dynamic address assignment).	Required	Yes
	8	ENTDAA, broadcast mode. (Enter dynamic address assignment).	Required	Yes

	9	DEFSLVS, broadcast mode. (Define list of slaves).		Optional	No
	10	SETMWL, broadcast mode. (Set Max Write Length).		Required	Yes
	11	SETMRL, broadcast mode. (Set Max Read Length).		Required	Yes
	12	ENTTM, broadcast mode. (Enter Test Mode).		Optional	No
	13	ENTHDR0, broadcast mode. (Enter HDR DDR mode)		Optional	Yes
	14	ENTHDR1, broadcast mode. (Enter HDR TSP mode)		Optional	No
	15	ENTHDR2, broadcast mode. (Enter HDR TSL mode)		Optional	No
	16	SETXTIME, broadcast mode. (Exchange Timing Information).			
		16.1	Defining byte = 0x7F (ST)	Optional	Yes
		16.2	Defining byte = 0xBF (DT)	Optional	Yes
		16.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
		16.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
		16.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
		16.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
		16.7	Defining byte = 0xFD (Async Trigger for Async Mode 3).	Optional	No
		16.8	Defining byte = 0x3F (TPH)	Optional	Yes
		16.9	Defining byte = 0x9f (TU)	Optional	Yes
		16.10	Defining byte = 0x8F (ODR)	Optional	Yes
	17	ENEC, direct mode. (Enable Events).		Required	Yes
	18	DISEC, direct mode. (Disable Events).		Required	Yes
	19	ENTAS0, direct mode. (Enter Activity State 0).		Required	Yes
	20	ENTAS1, direct mode. (Enter Activity State 1).		Optional	No
	21	ENTAS2, direct mode. (Enter Activity State 2).		Optional	No
	22	ENTAS3, direct mode. (Enter Activity State 3).		Optional	No
	23	RSTDAA, direct mode. (Reset dynamic address assignment).		Required	Yes
	24	SETDASA, direct mode. (Set Dynamic address from static address).		Optional	Yes

	25	SETNEWDA, direct mode. (Set new dynamic address)		Required	Yes
	26	SETMWL, direct mode. (Set Max Write Length).		Required / Conditional	Yes
	27	SETMRL, direct mode. (Set Max Read length).		Required / Conditional	Yes
	28	GETMWL, direct mode. (Get Max write length).		Required / Conditional	Yes
	29	GETMRL, direct mode. (Get Max Read length).		Required / Conditional	Yes
	30	GETPID, direct mode. (Get provisional ID).		Required	Yes
	31	GETBCR, direct mode. (Get Bus Characteristics Register).		Required	Yes
	32	GETDCR, direct mode. (Get Device Characteristics Register).		Required	Yes
	33	GETSTATUS, direct mode. (Get Device Status).		Required	Yes
	34	GETACCMST, direct mode. (Get Accept Mastership).		Optional	No
	35	SETBRGTGT, direct mode. (Set Bridge Targets).		Optional	No
	36	GETMXDS, direct mod. (Get Max Data Speed).		Optional	Yes
	37	GETHDRCAP, direct mode. (Get HDR capability).		Optional	Yes
	38	SETXTIME, direct mode. (Set Exchange Timing information).			
		38.1	Defining byte = 0x7F (ST)	Optional	Yes
		38.2	Defining byte = 0xBF (DT)	Optional	Yes
		38.3	Defining byte = 0xDF (Enter Async Mode 0)	Optional	Yes
		38.4	Defining byte = 0xEF (Enter Async Mode 1)	Optional	No
		38.5	Defining byte = 0xF7 (Enter Async Mode 2)	Optional	No
		38.6	Defining byte = 0xFB (Enter Async Mode 3)	Optional	No
		38.7	Defining byte = 0xFD (Async Trigger for Async Mode 3).	Optional	No
		38.8	Defining byte = 0x3F (TPH)	Optional	Yes
		38.9	Defining byte = 0x9f (TU)	Optional	Yes
		38.10	Defining byte = 0x8F (ODR)	Optional	Yes

	39	GETXTIME, direct mode. (Get Exchange Timing Information).	Optional	Yes

Table 13. I3C^{SM} CCC Commands

9.3 I^{2}C INTERFACE

I^{2}C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I^{2}C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-45608 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDDIO. The maximum bus speed is 1 MHz.

The slave address of the ICM-45608 is b110100X, which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AP_AD0. This allows two ICM-45608s to be connected to the same I^{2}C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AP_AD0 is logic low) and the address of the other should be b1101001 (pin AP_AD0 is logic high).

9.4 I^{2}C MASTER INTERFACE

I^{2}C master is compliant with the I^{2}C standard-Mode (max 100kbps), and I^{2}C Fast-Mode (max 400kbps). It supports 8-bit I^{2}C static address. It does not support multi-master on the I^{2}C bus. Clock-stretching by external I^{2}C devices is not supported.

9.5 SPI INTERFACE

The ICM-45608 supports 3-wire or 4-wire SPI for the host interface. The ICM-45608 always operates as a Slave device during standard Master-Slave SPI operation.

With respect to the Master, the Serial Clock output (SCLK), the Serial Data Output (SDO), the Serial Data Input (SDI), and the Serial Data IO (SDIO) are shared among the Slave devices. Each SPI slave device requires its own Chip Select (CS) line from the master.

CS goes low (active) at the start of transmission and goes back high (inactive) at the end. Only one CS line is active at a time, ensuring that only one slave is selected at any given time. The CS lines of the non-selected slave devices are held high, causing their SDO lines to remain in a high-impedance (high-z) state so that they do not interfere with any active devices.

SPI Operational Features

1. Data is delivered MSB first and LSB last
2. Data is latched on the rising edge of SCLK
3. Data should be transitioned on the falling edge of SCLK
4. The maximum frequency of SCLK is 24 MHz (it is 20MHz at VDDIO 1.2V)
5. SPI read and write operations are completed in 16 or more clock cycles (two or more bytes). The first byte contains the Register Address, and the following byte(s) contain(s) the SPI data. The first bit of the first byte contains the Read/Write bit and indicates the Read (1) operation. The following 7 bits contain the Register Address. In cases of multiple-byte Reads, data is two or more bytes:

Register Address format

MSB							**LSB**
R/W	A6	A5	A4	A3	A2	A1	A0

SPI Data format

MSB							**LSB**
D7	D6	D5	D4	D3	D2	D1	D0

6. Supports Single or Burst Read/Writes.

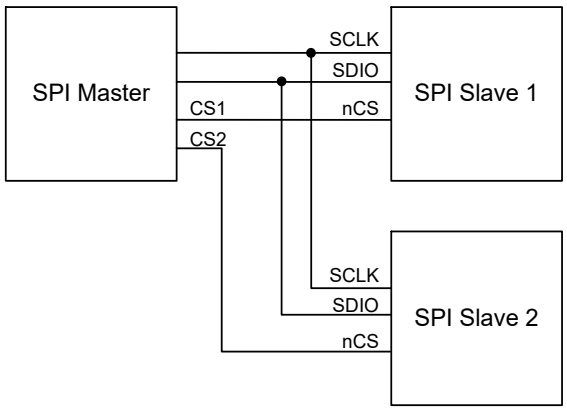

Figure 10. Typical SPI Master/Slave Configuration

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10 ASSEMBLY

This section provides general guidelines for assembling InvenSense Micro Electro-Mechanical Systems (MEMS) devices packaged in LGA package.

10.1 ORIENTATION OF AXES

The diagram below shows the orientation of the axes of sensitivity and the polarity of rotation. Note the pin 1 identifier (•) in the figure.

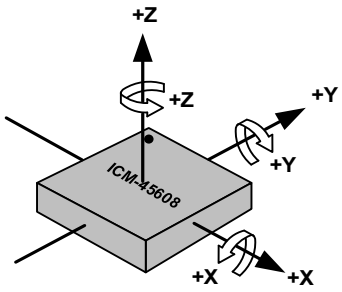
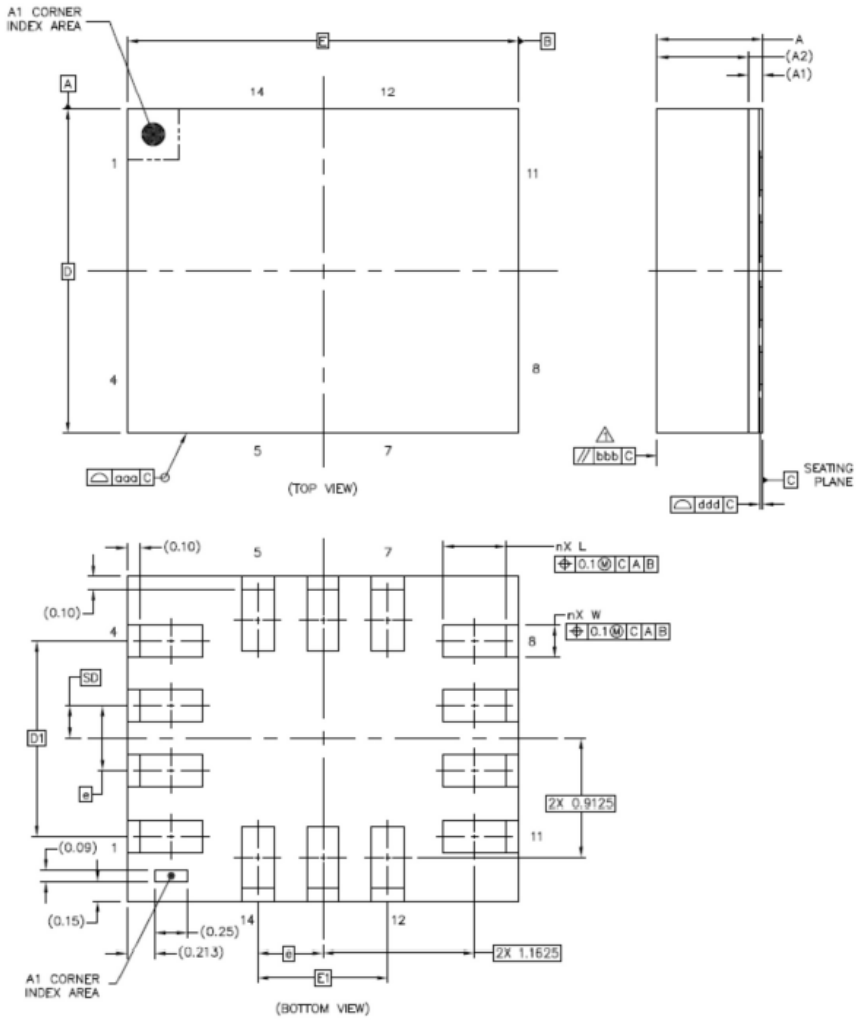


Figure 11. Orientation of Axes of Sensitivity and Polarity of Rotation

10.2 PACKAGE DIMENSIONS

14 Lead LGA (2.5x3x0.81) mm NiAu pad finish



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	SYMBOLS	DIMENSIONS IN MILLIMETERS		
		MIN	NOM	MAX
Total Thickness	A	0.76	0.81	0.86
Substrate Thickness	A1		0.105	REF
Mold Thickness	A2		0.7	REF
Body Size	D		2.5	BSC
	E		3	BSC
Lead Width	W	0.2	0.25	0.3
Lead Length	L	0.425	0.475	0.525
Lead Pitch	e		0.5	BSC
Lead Count	n		14	
Edge Ball Center to Center	D1		1.5	BSC
	E1		1	BSC
Body Center to Contact Ball	SD		0.25	BSC
	SE		---	BSC
Package Edge Tolerance	aaa		0.1	
Mold Flatness	bbb		0.2	
Coplanarity	ddd		0.08	

11 DEVICE PACKAGE IN TAPE AND REEL

ICM-45608 devices are packaged in the tape and reel as shown in the figures below.

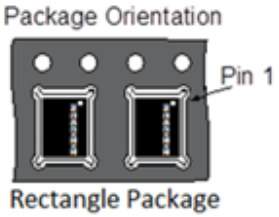

Figure 12. ICM-45608 Device Package in Tape and Reel

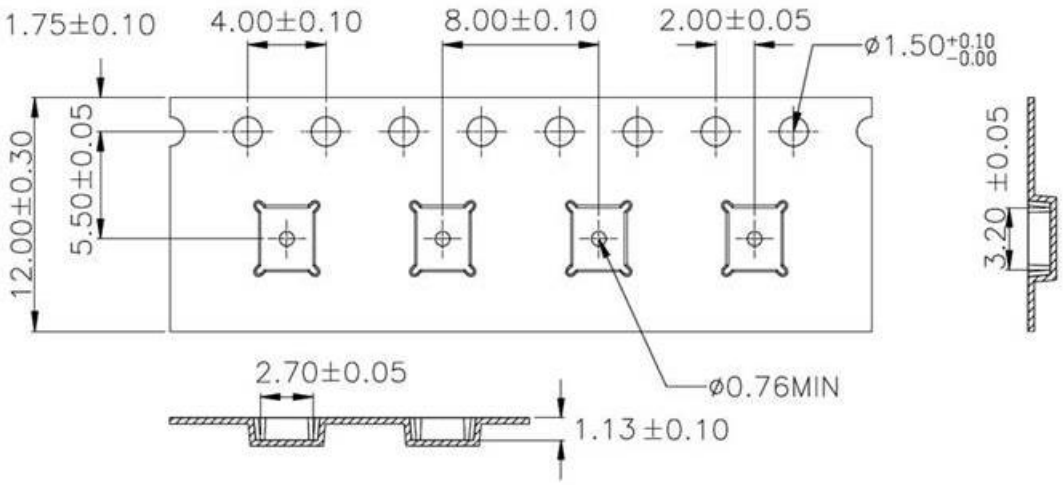

Figure 13. Tape Dimensions with ICM-45608 Device Package

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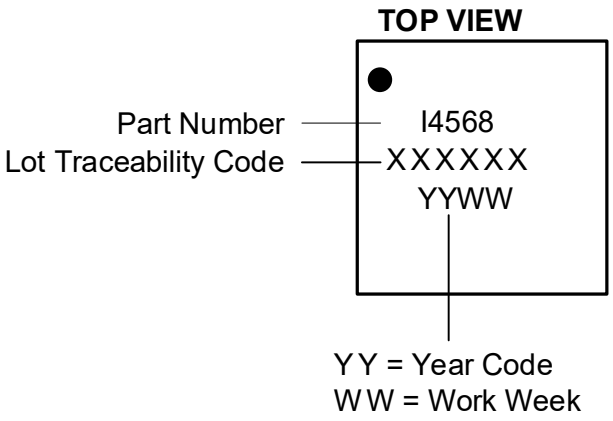
12 PART NUMBER PACKAGE MARKING

The part number package marking for ICM-45608 devices is summarized below:

Part Number	Part Number Package Marking
ICM-45608	I4568



13 INDIRECT REGISTER ACCESS

13.1 HOST INDIRECT ACCESS REGISTER (IREG)

An IREG is a register or a memory storage element that is not addressed directly by a 7-bit address. IREGs can only be addressed using an internal 16-bit address. Indirect register access procedures described in this section must be used to access all IREGs.

The host configures the internal 16-bit address by programming following registers:
{ireg_addr_15_8[7:0], ireg_addr_7_0[7:0]}.

13.2 GENERAL RULES FOR ACCESSING IREG

1. Burst-write and burst-read operations are not supported when accessing IREGs from the host.
2. Reading of an IREG is done on a read-pre-fetch basis (details in IREG READ section below).
3. A minimum wait time (refer to section MINIMUM WAIT TIME GAP below for details) is required between two consecutive read/write access to an IREG.

13.3 MINIMUM WAIT TIME-GAP

The minimum time gap between two consecutive IREG accesses for various IREG components is 4µs.

13.4 IREG WRITE

Procedure for writing to an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_APEX, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_APEX registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. The host programs the write data to the IREG_DATA register.
3. The above programming steps must be performed in a single burst-write transaction to prevent an un-intended read-pre-fetch operation.
4. After the IREG_DATA register is written, an internal operation is triggered to pass the contents from the IREG_DATA register to a register pointed by {IREG_ADDR_7_0, IREG_ADDR_15_8}.
5. After the contents from the IREG_DATA register is written to the selected register, the internal 16-bit address is auto-incremented.

6. After a minimum wait time-gap, the host can write to the IREG_DATA register again, which is effectively writing to the register pointed by the post-auto-incremented address.
7. Or, after a minimum wait time-gap, the host can program a new destination address for the next write operation.

13.5 IREG READ

Procedure for reading from an IREG.

1. The host specifies the destination address of an IREG by programming IREG_ADDR_7_0, IREG_ADDR_15_8.
    a. If host wants to access a register in IMEM_SRAM, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    b. If host wants to access a register in IMEM_SRAM_APEX, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_APEX registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    c. If host wants to access a register in IMEM_SRAM_STC, it should add base address 0x0000 to the address of that register shown in the IMEM_SRAM_STC registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    d. If host wants to access a register in IPREG_BAR, it should add base address 0xA000 to the address of that register shown in the IPREG_BAR registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    e. If host wants to access a register in IPREG_SYS1, it should add base address 0xA400 to the address of that register shown in the IPREG_SYS1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    f. If host wants to access a register in IPREG_SYS2, it should add base address 0xA500 to the address of that register shown in the IPREG_SYS2 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
    g. If host wants to access a register in IPREG_TOP1, it should add base address 0xA200 to the address of that register shown in the IPREG_TOP1 registers section, and then use that resulting value in registers IREG_ADDR_7_0, IREG_ADDR_15_8.
2. Upon the CSB=1 (SPI) or STOP (I2C) after the above programming, an internal read-pre-fetch operation is triggered.
3. The internal read-pre-fetch operation returns the desired data, which is saved to the IREG_DATA register.
4. After a minimum wait time-gap, the host reads the IREG_DATA register to retrieve the read-data.
5. After the host reads the IREG_DATA register, the internal 16-bit address is auto-incremented, and another internal read-pre-fetch is automatically triggered, to fetch data from the IREG register pointed to by the post-auto-incremented address.
6. After a minimum wait time-gap, the host can either read the IREG_DATA register to get the read-data from the next address location, or it can program a new read address.

14 DEVICE CONFIGURATION FOR DATA ENDIANNESS

By default the device data endianness is Little Endian, for data in Sensor Data Registers and FIFO, and for FIFO Count. User must set register field SREG_DATA_ENDIAN_SEL in register SREG_CTRL to 1, to enable Big Endian data format for data in Sensor Data Registers and FIFO, and for FIFO Count.

Data descriptions in the register map for Sensor Data Registers, FIFO data, and FIFO Count are for the commonly used Big Endian format.

15 REGISTER MAP

This section lists the register map for the ICM-45608, for user bank 0, IMEM_SRAM, IPREG_BAR, IPREG_TOP1, IPREG_SYS1, IPREG_SYS2.

Please refer to the procedure in Section 14 for configuring device data endianness before using the register map.

15.1 USER BANK 0 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	ACCEL_DATA_X1_UI	SYNCR	ACCEL_DATA_X_UI[15:8]							
01	01	ACCEL_DATA_X0_UI	SYNCR	ACCEL_DATA_X_UI[7:0]							
02	02	ACCEL_DATA_Y1_UI	SYNCR	ACCEL_DATA_Y_UI[15:8]							
03	03	ACCEL_DATA_Y0_UI	SYNCR	ACCEL_DATA_Y_UI[7:0]							
04	04	ACCEL_DATA_Z1_UI	SYNCR	ACCEL_DATA_Z_UI[15:8]							
05	05	ACCEL_DATA_Z0_UI	SYNCR	ACCEL_DATA_Z_UI[7:0]							
06	06	GYRO_DATA_X1_UI	SYNCR	GYRO _DATA_X_UI[15:8]							
07	07	GYRO _DATA_X0_UI	SYNCR	GYRO _DATA_X_UI[7:0]							
08	08	GYRO _DATA_Y1_UI	SYNCR	GYRO _DATA_Y_UI[15:8]							
09	09	GYRO _DATA_Y0_UI	SYNCR	GYRO _DATA_Y_UI[7:0]							
0A	10	GYRO _DATA_Z1_UI	SYNCR	GYRO_DATA_Z_UI[15:8]							
0B	11	GYRO _DATA_Z0_UI	SYNCR	GYRO_DATA_Z_UI[7:0]							
0C	12	TEMP_DATA1_UI	SYNCR	TEMP_DATA_UI[15:8]							
0D	13	TEMP_DATA0_UI	SYNCR	TEMP_DATA_UI[7:0]							
0E	14	TMST_FSYNCH	SYNCR	TMST_FSYNC_DATA_UI[15:8]							
0F	15	TMST_FSYNCL	SYNCR	TMST_FSYNC_DATA_UI[7:0]							
10	16	PWR_MGMT0	R/W	-				GYRO_MODE		ACCEL_MODE	
12	18	FIFO_COUNT_0	R	FIFO_DATA_CNT[15:8]							
13	19	FIFO_COUNT_1	R	FIFO_DATA_CNT[7:0]							
14	20	FIFO_DATA	R	FIFO_DATA							
16	22	INT1_CONFIG0	R/W	INT1_STATUS_EN_RESET_DONE	INT1_STATUS_EN_AUX1_AGC_RDY	INT1_STATUS_EN_AP_AGC_RDY	INT1_STATUS_EN_AP_FSYNC	INT1_STATUS_EN_AUX1_DRDY	INT1_STATUS_EN_DRDY	INT1_STATUS_EN_FIFO_THS	INT1_STATUS_EN_FIFO_FULL
17	23	INT1_CONFIG1	R/W	-	INT1_STATUS_EN_APEX_EVENT	INT1_STATUS_EN_I2CM_DONE	INT1_STATUS_EN_I3C_PROTOCOL_ERR	INT1_STATUS_EN_WOM_Z	INT1_STATUS_EN_WOM_Y	INT1_STATUS_EN_WOM_X	INT1_STATUS_EN_PLL_RDY
18	24	INT1_CONFIG2	R/W	-					INT1_DRIVE	INT1_MODE	INT1_POLARITY
19	25	INT1_STATUS0	R/C	INT1_STATUS_RESET_DONE	INT1_STATUS_AUX1_AGC_RDY	INT1_STATUS_AP_AGC_RDY	INT1_STATUS_AP_FSYNC	INT1_STATUS_AUX1_DRDY	INT1_STATUS_DRDY	INT1_STATUS_FIFO_THS	INT1_STATUS_FIFO_FULL
1A	26	INT1_STATUS1	R/C	-	INT1_STATUS_APEX_EVENT	INT1_STATUS_I2CM_DONE	INT1_STATUS_I3C_PROTOCOL_ERR	INT1_STATUS_WOM_Z	INT1_STATUS_WOM_Y	INT1_STATUS_WOM_X	INT1_STATUS_PLL_RDY
1B	27	ACCEL_CONFIG0	R/W	-	ACCEL_UI_FS_SEL			ACCEL_ODR			
1C	28	GYRO_CONFIG0	R/W	GYRO_UI_FS_SEL				GYRO_ODR			
1D	29	FIFO_CONFIG0	R/W	FIFO_MODE		FIFO_DEPTH					
1E	30	FIFO_CONFIG1_0	R/W	FIFO_WM_TH[7:0]							
1F	31	FIFO_CONFIG1_1	R/W	FIFO_WM_TH[15:8]							
20	32	FIFO_CONFIG2	R/W	FIFO_FLUSH	-			FIFO_WR_WM_GT_TH	-		
21	33	FIFO_CONFIG3	R/W	-		FIFO_ES1_EN	FIFO_ES0_EN	FIFO_HIRES_EN	FIFO_GYRO_EN	FIFO_ACCEL_EN	FIFO_IF_EN
22	34	FIFO_CONFIG4	R/W	-		FIFO_COMP_NC_FLOW_CFG			FIFO_COMP_EN	FIFO_TMST_FSYNC_EN	FIFO_ES0_6B_9B
23	35	TMST_WOM_CONFIG	R/W	-	TMST_DELTA_EN	TMST_RESOL	WOM_EN	WOM_MODE	WOM_INT_MODE	WOM_INT_DUR	

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
24	36	FSYNC_CONFIG0	R/W	-				AP_FSYNC_FLAG_CLEAR_SEL	AP_FSYNC_SEL		
27	39	DMP_EXT_SEN_ODR_CFG	R/W	-	EXT_SENSOR_EN	EXT_ODR			APEX_ODR		
28	40	ODR_DECIMATE_CONFIG	R/W	GYRO_FIFO_ODR_DEC				ACCEL_FIFO_ODR_DEC			
29	41	EDMP_APEX_EN0	R/W	RESERVED4	RESERVED3	FF_EN	RESERVED2	RESERVED1	RESERVED0	SIF_EN	TAP_EN
2A	42	EDMP_APEX_EN1	R/W	-	EDMP_ENABLE	FEATURE3_EN	GAF_EN	-	POWER_SAVE_EN	INIT_EN	SOFT_HARD_IRON_CORR_EN
2B	43	APEX_BUFFER_MGMT	R/W	FF_DURATION_HOST_RPTR		FF_DURATION_EDMP_WPTR		-			
2C	44	INTF_CONFIG0	R/W	-						AP_SPI_34_MODE	AP_SPI_MODE
2D	45	INTF_CONFIG1_OVRD	R/W	-				AP_SPI_34_MODE_OVRD	AP_SPI_34_MODE_OVRD_VAL	AP_SPI_MODE_OVRD	AP_SPI_MODE_OVRD_VAL
2F	47	IOC_PAD_SCENARIO	R	-					AUX1_MODE		AUX1_ENABLE
30	48	IOC_PAD_SCENARIO_AUX_OVRD	R/W	-			AUX1_MODE_OVRD	AUX1_ENABLE_OVRD_VAL		AUX1_ENABLE_OVRD	AUX1_ENABLE_OVRD_VAL
32	50	DRIVE_CONFIG0	R/W	-	PADS_I2C_SLEW			PADS_SPI_SLEW			-
33	51	DRIVE_CONFIG1	R/W	-		PADS_I3C_DDR_SLEW			PADS_I3C_SDR_SLEW		
34	52	DRIVE_CONFIG2	R/W	-					PADS_SLEW		
39	57	INT_APEX_CONFIG0	R/W	INT_STATUS_MASK_PIN_EXT2_DET	INT_STATUS_MASK_PIN_FF_DET	INT_STATUS_MASK_PIN_EXT1_DET	INT_STATUS_MASK_PIN_EXT0_DET	INT_STATUS_MASK_PIN_SIF_DET	INT_STATUS_MASK_PIN_LOW_G_DET	INT_STATUS_MASK_PIN_HIGH_G_DET	INT_STATUS_MASK_PIN_TAP_DET
3A	58	INT_APEX_CONFIG1	R/W	-	INT_STATUS_MASK_PIN_EXT6_DET	INT_STATUS_MASK_PIN_EXT5_DET	INT_STATUS_MASK_PIN_SA_DONE	-	INT_STATUS_MASK_PIN_SELFTEST_DONE	INT_STATUS_MASK_PIN_EXT4_DET	INT_STATUS_MASK_PIN_EXT3_DET
3B	59	INT_APEX_STATUS0	R/C	INT_STATUS_EXT2_DET	INT_STATUS_FF_DET	INT_STATUS_EXT1_DET	INT_STATUS_EXT0_DET	INT_STATUS_SIF_DET	INT_STATUS_LOW_G_DET	INT_STATUS_HIGH_G_DET	INT_STATUS_TAP_DET
3C	60	INT_APEX_STATUS1	R/C	-	INT_STATUS_EXT6_DET	INT_STATUS_EXT5_DET	INT_STATUS_SA_DONE	-	INT_STATUS_SELFTEST_DONE	INT_STATUS_EXT4_DET	INT_STATUS_EXT3_DET
56	86	INT2_CONFIG0	R/W	INT2_STATUS_EN_RESET_DONE	INT2_STATUS_EN_AUX1_AGC_RDY	INT2_STATUS_EN_AP_AGC_RDY	INT2_STATUS_EN_AP_FSYNC	INT2_STATUS_EN_AUX1_DRDY	INT2_STATUS_EN_DRDY	INT2_STATUS_EN_FIFO_THS	INT2_STATUS_EN_FIFO_FULL
57	87	INT2_CONFIG1	R/W	-	INT2_STATUS_EN_APEX_EVENT	INT2_STATUS_EN_I2CM_DONE	INT2_STATUS_EN_I3C_PROTOCOL_ERR	INT2_STATUS_EN_WOM_Z	INT2_STATUS_EN_WOM_Y	INT2_STATUS_EN_WOM_X	INT2_STATUS_EN_PLL_RDY
58	88	INT2_CONFIG2	R/W	-					INT2_DRIVE	INT2_MODE	INT2_POLARITY
59	89	INT2_STATUS0	R/C	INT2_STATUS_RESET_DONE	INT2_STATUS_AUX1_AGC_RDY	INT2_STATUS_AP_AGC_RDY	INT2_STATUS_AP_FSYNC	INT2_STATUS_AUX1_DRDY	INT2_STATUS_DRDY	INT2_STATUS_FIFO_THS	INT2_STATUS_FIFO_FULL
5A	90	INT2_STATUS1	R/C	-	INT2_STATUS_APEX_EVENT	INT2_STATUS_I2CM_DONE	INT2_STATUS_I3C_PROTOCOL_ERR	INT2_STATUS_WOM_Z	INT2_STATUS_WOM_Y	INT2_STATUS_WOM_X	INT2_STATUS_PLL_RDY
72	114	WHO_AM_I	R	WHOAMI							
73	115	REG_HOST_MSG	R/W	-		EDMP_ON_DEMAND_EN	-				TESTOPENABLE
7C	124	IREG_ADDR_15_8	R/W	IREG_ADDR_15_8							
7D	125	IREG_ADDR_7_0	R/W	IREG_ADDR_7_0							
7E	126	IREG_DATA	R/W	IREG_DATA							
7F	127	REG_MISC2	R/W	-						SOFT_RST	IREG_DONE

15.2 USER BANK IMEM_SRAM REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00	00	IMEM_SRAM_REG_0	R/W	GYRO_X_STR_FT[7:0]							
01	01	IMEM_SRAM_REG_1	R/W	GYRO_X_STR_FT[15:8]							
02	02	IMEM_SRAM_REG_2	R/W	GYRO_Y_STR_FT[7:0]							
03	03	IMEM_SRAM_REG_3	R/W	GYRO_Y_STR_FT[15:8]							
04	04	IMEM_SRAM_REG_4	R/W	GYRO_Z_STR_FT[7:0]							
05	05	IMEM_SRAM_REG_5	R/W	GYRO_Z_STR_FT[15:8]							
06	06	IMEM_SRAM_REG_6	R/W	GYRO_X_CMOS_GAIN_FT[7:0]							
07	07	IMEM_SRAM_REG_7	R/W	-				GYRO_X_CMOS_GAIN_FT[11:8]			
08	08	IMEM_SRAM_REG_8	R/W	GYRO_Y_CMOS_GAIN_FT[7:0]							
09	09	IMEM_SRAM_REG_9	R/W	-				GYRO_Y_CMOS_GAIN_FT[11:8]			
0A	10	IMEM_SRAM_REG_10	R/W	GYRO_Z_CMOS_GAIN_FT[7:0]							
0B	11	IMEM_SRAM_REG_11	R/W	-				GYRO_Z_CMOS_GAIN_FT[11:8]			
0C	12	IMEM_SRAM_REG_12	R/W	ACCEL_X_STR_FT[7:0]							
0D	13	IMEM_SRAM_REG_13	R/W	ACCEL_X_STR_FT[15:8]							
0E	14	IMEM_SRAM_REG_14	R/W	ACCEL_Y_STR_FT[7:0]							
0F	15	IMEM_SRAM_REG_15	R/W	ACCEL_Y_STR_FT[15:8]							
10	16	IMEM_SRAM_REG_16	R/W	ACCEL_Z_STR_FT[7:0]							
11	17	IMEM_SRAM_REG_17	R/W	ACCEL_Z_STR_FT[15:8]							

15.3 USER BANK IMEM_SRAM_APEX REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04	04	IMEM_SRAM_APEX_REG_4	R/W	ONDEMAND_DYNAMIC_SERVICE_REQUEST[7:0]							
05	05	IMEM_SRAM_APEX_REG_5	R/W	USE_CASE_BITMASK[7:0]							
07	07	IMEM_SRAM_APEX_REG_7	R/W	TAP_NUM[7:0]							
08	08	IMEM_SRAM_APEX_REG_8	R/W	TAP_AXIS[7:0]							
09	09	IMEM_SRAM_APEX_REG_9	R/W	TAP_DIR[7:0]							
40	64	IMEM_SRAM_APEX_REG_64	R/W	POWER_SAVE_TIME[7:0]							
41	65	IMEM_SRAM_APEX_REG_65	R/W	POWER_SAVE_TIME[15:8]							
42	66	IMEM_SRAM_APEX_REG_66	R/W	POWER_SAVE_TIME[23:16]							
43	67	IMEM_SRAM_APEX_REG_67	R/W	POWER_SAVE_TIME[31:24]							
118	280	IMEM_SRAM_APEX_REG_280	R/W	ONDEMAND_STATIC_SERVICE_REQUEST[7:0]							
119	281	IMEM_SRAM_APEX_REG_281	R/W	ONDEMAND_STATIC_SERVICE_REQUEST[15:8]							
11A	282	IMEM_SRAM_APEX_REG_282	R/W	ONDEMAND_STATIC_SERVICE_REQUEST[23:16]							
11B	283	IMEM_SRAM_APEX_REG_283	R/W	ONDEMAND_STATIC_SERVICE_REQUEST[31:24]							
11C	284	IMEM_SRAM_APEX_REG_284	R/W	ONDEMAND_MEMSET_ADDR[7:0]							
11D	285	IMEM_SRAM_APEX_REG_285	R/W	ONDEMAND_MEMSET_ADDR[15:8]							
11E	286	IMEM_SRAM_APEX_REG_286	R/W	ONDEMAND_MEMSET_VALUE[7:0]							
120	288	IMEM_SRAM_APEX_REG_288	R/W	ONDEMAND_MEMSET_SIZE[7:0]							
121	289	IMEM_SRAM_APEX_REG_289	R/W	ONDEMAND_MEMSET_SIZE[15:8]							
138	312	IMEM_SRAM_APEX_REG_312	R/W	SIF_PDR_PARTITION[7:0]							
139	313	IMEM_SRAM_APEX_REG_313	R/W	SIF_PDR_PARTITION[15:8]							
13A	314	IMEM_SRAM_APEX_REG_314	R/W	SIF_PDR_PARTITION[23:16]							
13B	315	IMEM_SRAM_APEX_REG_315	R/W	SIF_PDR_PARTITION[31:24]							
154	340	IMEM_SRAM_APEX_REG_340	R/W	GAF_PDR_PARTITION[7:0]							
155	341	IMEM_SRAM_APEX_REG_341	R/W	GAF_PDR_PARTITION15:8]							
156	342	IMEM_SRAM_APEX_REG_342	R/W	GAF_PDR_PARTITION[23:16]							
157	343	IMEM_SRAM_APEX_REG_343	R/W	GAF_PDR_PARTITION[31:24]							
188	392	IMEM_SRAM_APEX_REG_392	R/W	DMP_ODR_LAST_INIT[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
189	393	IMEM_SRAM_APEX_REG_393	R/W	DMP_ODR_LAST_INIT[15:8]							
18A	394	IMEM_SRAM_APEX_REG_394	R/W	DMP_ODR_LAST_INIT[23:16]							
18B	395	IMEM_SRAM_APEX_REG_395	R/W	DMP_ODR_LAST_INIT[31:24]							
1AC	428	IMEM_SRAM_APEX_REG_428	R/W	GLOBAL_MOUNTING_MATRIX[7:0]							
1AD	429	IMEM_SRAM_APEX_REG_429	R/W	GLOBAL_MOUNTING_MATRIX[15:8]							
1AE	430	IMEM_SRAM_APEX_REG_430	R/W	GLOBAL_MOUNTING_MATRIX[23:16]							
1AF	431	IMEM_SRAM_APEX_REG_431	R/W	GLOBAL_MOUNTING_MATRIX[31:24]							
1B0	432	IMEM_SRAM_APEX_REG_432	R/W	GLOBAL_MOUNTING_MATRIX[39:32]							
1B1	433	IMEM_SRAM_APEX_REG_433	R/W	GLOBAL_MOUNTING_MATRIX[47:40]							
1B2	434	IMEM_SRAM_APEX_REG_434	R/W	GLOBAL_MOUNTING_MATRIX[55:48]							
1B3	435	IMEM_SRAM_APEX_REG_435	R/W	GLOBAL_MOUNTING_MATRIX[63:56]							
1B4	436	IMEM_SRAM_APEX_REG_436	R/W	GLOBAL_MOUNTING_MATRIX[71:64]							
1B5	437	IMEM_SRAM_APEX_REG_437	R/W	GLOBAL_MOUNTING_MATRIX[79:72]							
1B6	438	IMEM_SRAM_APEX_REG_438	R/W	GLOBAL_MOUNTING_MATRIX[87:80]							
1B7	439	IMEM_SRAM_APEX_REG_439	R/W	GLOBAL_MOUNTING_MATRIX[95:88]							
1B8	440	IMEM_SRAM_APEX_REG_440	R/W	GLOBAL_MOUNTING_MATRIX[103:96]							
1B9	441	IMEM_SRAM_APEX_REG_441	R/W	GLOBAL_MOUNTING_MATRIX[111:104]							
1BA	442	IMEM_SRAM_APEX_REG_442	R/W	GLOBAL_MOUNTING_MATRIX[119:112]							
1BB	443	IMEM_SRAM_APEX_REG_443	R/W	GLOBAL_MOUNTING_MATRIX[127:120]							
1BC	444	IMEM_SRAM_APEX_REG_444	R/W	GLOBAL_MOUNTING_MATRIX[135:128]							
1BD	445	IMEM_SRAM_APEX_REG_445	R/W	GLOBAL_MOUNTING_MATRIX[143:136]							
1BE	446	IMEM_SRAM_APEX_REG_446	R/W	GAF_MODE[7:0]							
1C1	449	IMEM_SRAM_APEX_REG_449	R/W	GAF_ONDEMAND_MRM_REQUEST[7:0]							
202	514	IMEM_SRAM_APEX_REG_514	R/W	FF_DURATION[7:0]							
203	515	IMEM_SRAM_APEX_REG_515	R/W	FF_DURATION[15:8]							
208	520	IMEM_SRAM_APEX_REG_520	R/W	FF_MIN_DURATION[7:0]							
209	521	IMEM_SRAM_APEX_REG_521	R/W	FF_MIN_DURATION[15:8]							
20A	522	IMEM_SRAM_APEX_REG_522	R/W	FF_MIN_DURATION[23:16]							
20B	523	IMEM_SRAM_APEX_REG_523	R/W	FF_MIN_DURATION[31:24]							
20C	524	IMEM_SRAM_APEX_REG_524	R/W	FF_MAX_DURATION[7:0]							
20D	525	IMEM_SRAM_APEX_REG_525	R/W	FF_MAX_DURATION[15:8]							
20E	526	IMEM_SRAM_APEX_REG_526	R/W	FF_MAX_DURATION[23:16]							
20F	527	IMEM_SRAM_APEX_REG_527	R/W	FF_MAX_DURATION[31:24]							
210	528	IMEM_SRAM_APEX_REG_528	R/W	FF_DEBOUNCE_DURATION[7:0]							
211	529	IMEM_SRAM_APEX_REG_529	R/W	FF_DEBOUNCE_DURATION[15:8]							
212	530	IMEM_SRAM_APEX_REG_530	R/W	FF_DEBOUNCE_DURATION[23:16]							
213	531	IMEM_SRAM_APEX_REG_531	R/W	FF_DEBOUNCE_DURATION[31:24]							
218	536	IMEM_SRAM_APEX_REG_536	R/W	HIGHG_PEAK_TH[7:0]							
219	537	IMEM_SRAM_APEX_REG_537	R/W	HIGHG_PEAK_TH[15:8]							
21A	538	IMEM_SRAM_APEX_REG_538	R/W	HIGHG_PEAK_TH_HYST[7:0]							
21B	539	IMEM_SRAM_APEX_REG_539	R/W	HIGHG_PEAK_TH_HYST[15:8]							
21C	540	IMEM_SRAM_APEX_REG_540	R/W	HIGHG_TIME_TH[7:0]							
21D	541	IMEM_SRAM_APEX_REG_541	R/W	HIGHG_TIME_TH[15:8]							
224	548	IMEM_SRAM_APEX_REG_548	R/W	LOWG_PEAK_TH[7:0]							
225	549	IMEM_SRAM_APEX_REG_549	R/W	LOWG_PEAK_TH[15:8]							
226	550	IMEM_SRAM_APEX_REG_550	R/W	LOWG_PEAK_TH_HYST[7:0]							
227	551	IMEM_SRAM_APEX_REG_551	R/W	LOWG_PEAK_TH_HYST[15:8]							
228	552	IMEM_SRAM_APEX_REG_552	R/W	LOWG_TIME_TH[7:0]							
229	553	IMEM_SRAM_APEX_REG_553	R/W	LOWG_TIME_TH[15:8]							
230	560	IMEM_SRAM_APEX_REG_560	R/W	TAP_MIN_JERK[7:0]							
231	561	IMEM_SRAM_APEX_REG_561	R/W	TAP_MIN_JERK[15:8]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
232	562	IMEM_SRAM_APEX_REG_562	R/W	TAP_TMAX[7:0]							
233	563	IMEM_SRAM_APEX_REG_563	R/W	TAP_TMAX[15:8]							
234	564	IMEM_SRAM_APEX_REG_564	R/W	TAP_TMIN[7:0]							
235	565	IMEM_SRAM_APEX_REG_565	R/W	TAP_SMUDGE_REJECT_THR[7:0]							
236	566	IMEM_SRAM_APEX_REG_566	R/W	TAP_MAX_PEAK_TOL[7:0]							
237	567	IMEM_SRAM_APEX_REG_567	R/W	TAP_TAVG[7:0]							
238	568	IMEM_SRAM_APEX_REG_568	R/W	TAP_ODR[7:0]							
239	569	IMEM_SRAM_APEX_REG_569	R/W	TAP_MAX[7:0]							
23A	570	IMEM_SRAM_APEX_REG_570	R/W	TAP_MIN[7:0]							
264	612	IMEM_SRAM_APEX_REG_612	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[7:0]							
265	613	IMEM_SRAM_APEX_REG_613	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[15:8]							
266	614	IMEM_SRAM_APEX_REG_614	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[23:16]							
267	615	IMEM_SRAM_APEX_REG_615	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[31:24]							
268	616	IMEM_SRAM_APEX_REG_616	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[39:32]							
269	617	IMEM_SRAM_APEX_REG_617	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[47:40]							
26A	618	IMEM_SRAM_APEX_REG_618	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[55:48]							
26B	619	IMEM_SRAM_APEX_REG_619	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[63:56]							
26C	620	IMEM_SRAM_APEX_REG_620	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[71:64]							
26D	621	IMEM_SRAM_APEX_REG_621	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[79:72]							
26E	622	IMEM_SRAM_APEX_REG_622	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[87:80]							
26F	623	IMEM_SRAM_APEX_REG_623	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[95:88]							
270	624	IMEM_SRAM_APEX_REG_624	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[103:96]							
271	625	IMEM_SRAM_APEX_REG_625	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[111:104]							
272	626	IMEM_SRAM_APEX_REG_626	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[119:112]							
273	627	IMEM_SRAM_APEX_REG_627	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[127:120]							
274	628	IMEM_SRAM_APEX_REG_628	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[135:128]							
275	629	IMEM_SRAM_APEX_REG_629	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[143:136]							
276	630	IMEM_SRAM_APEX_REG_630	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[151:144]							
277	631	IMEM_SRAM_APEX_REG_631	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[159:152]							
278	632	IMEM_SRAM_APEX_REG_632	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[167:160]							
279	633	IMEM_SRAM_APEX_REG_633	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[175:168]							
27A	634	IMEM_SRAM_APEX_REG_634	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[183:176]							
27B	635	IMEM_SRAM_APEX_REG_635	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[191:184]							
27C	636	IMEM_SRAM_APEX_REG_636	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[199:192]							
27D	637	IMEM_SRAM_APEX_REG_637	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[207:200]							
27E	638	IMEM_SRAM_APEX_REG_638	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[215:208]							
27F	639	IMEM_SRAM_APEX_REG_639	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[223:216]							
280	640	IMEM_SRAM_APEX_REG_640	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[231:224]							
281	641	IMEM_SRAM_APEX_REG_641	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[239:232]							
282	642	IMEM_SRAM_APEX_REG_642	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[247:240]							
283	643	IMEM_SRAM_APEX_REG_643	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[255:248]							
284	644	IMEM_SRAM_APEX_REG_644	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[263:256]							
285	645	IMEM_SRAM_APEX_REG_645	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[271:264]							
286	646	IMEM_SRAM_APEX_REG_646	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[279:272]							
287	647	IMEM_SRAM_APEX_REG_647	R/W	GAF_CONFIG_MAG_SOFTIRON_MATRIX[287:280]							
288	648	IMEM_SRAM_APEX_REG_648	R/W	GAF_CONFIG_ACC_ODR_US[7:0]							
289	649	IMEM_SRAM_APEX_REG_649	R/W	GAF_CONFIG_ACC_ODR_US[15:8]							
28A	650	IMEM_SRAM_APEX_REG_650	R/W	GAF_CONFIG_ACC_ODR_US[23:16]							
28B	651	IMEM_SRAM_APEX_REG_651	R/W	GAF_CONFIG_ACC_ODR_US[31:24]							
28C	652	IMEM_SRAM_APEX_REG_652	R/W	GAF_CONFIG_GYR_ODR_US[7:0]							
28D	653	IMEM_SRAM_APEX_REG_653	R/W	GAF_CONFIG_GYR_ODR_US[15:8]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
28E	654	IMEM_SRAM_APEX_REG_654	R/W	GAF_CONFIG_GYR_ODR_US[23:16]							
28F	655	IMEM_SRAM_APEX_REG_655	R/W	GAF_CONFIG_GYR_ODR_US[31:24]							
290	656	IMEM_SRAM_APEX_REG_656	R/W	GAF_CONFIG_ACC_PDR_US[7:0]							
291	657	IMEM_SRAM_APEX_REG_657	R/W	GAF_CONFIG_ACC_PDR_US[15:8]							
292	658	IMEM_SRAM_APEX_REG_658	R/W	GAF_CONFIG_ACC_PDR_US[23:16]							
293	659	IMEM_SRAM_APEX_REG_659	R/W	GAF_CONFIG_ACC_PDR_US[31:24]							
294	660	IMEM_SRAM_APEX_REG_660	R/W	GAF_CONFIG_GYR_PDR_US[7:0]							
295	661	IMEM_SRAM_APEX_REG_661	R/W	GAF_CONFIG_GYR_PDR_US[15:8]							
296	662	IMEM_SRAM_APEX_REG_662	R/W	GAF_CONFIG_GYR_PDR_US[23:16]							
297	663	IMEM_SRAM_APEX_REG_663	R/W	GAF_CONFIG_GYR_PDR_US[31:24]							
298	664	IMEM_SRAM_APEX_REG_664	R/W	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[7:0]							
299	665	IMEM_SRAM_APEX_REG_665	R/W	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[15:8]							
29A	666	IMEM_SRAM_APEX_REG_666	R/W	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[23:16]							
29B	667	IMEM_SRAM_APEX_REG_667	R/W	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[31:24]							
29C	668	IMEM_SRAM_APEX_REG_668	R/W	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[7:0]							
29D	669	IMEM_SRAM_APEX_REG_669	R/W	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[15:8]							
29E	670	IMEM_SRAM_APEX_REG_670	R/W	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[23:16]							
29F	671	IMEM_SRAM_APEX_REG_671	R/W	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[31:24]							
2A0	672	IMEM_SRAM_APEX_REG_672	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[7:0]							
2A1	673	IMEM_SRAM_APEX_REG_673	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[15:8]							
2A2	674	IMEM_SRAM_APEX_REG_674	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[23:16]							
2A3	675	IMEM_SRAM_APEX_REG_675	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[31:24]							
2A4	676	IMEM_SRAM_APEX_REG_676	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[7:0]							
2A5	677	IMEM_SRAM_APEX_REG_677	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[15:8]							
2A6	678	IMEM_SRAM_APEX_REG_678	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[23:16]							
2A7	679	IMEM_SRAM_APEX_REG_679	R/W	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[31:24]							
2AC	684	IMEM_SRAM_APEX_REG_684	R/W	GAF_CONFIG_PLL_CLOCK_VARIATION[7:0]							
2AD	685	IMEM_SRAM_APEX_REG_685	R/W	GAF_CONFIG_STATIONARY_ANGLE_ENABLE[7:0]							
2AE	686	IMEM_SRAM_APEX_REG_686	R/W	GAF_CONFIG_RUN_SPHERICAL[7:0]							
4A0	1184	IMEM_SRAM_APEX_REG_1184	R/W	GAF_CONFIG_GYR_DT_US[7:0]							
4A1	1185	IMEM_SRAM_APEX_REG_1185	R/W	GAF_CONFIG_GYR_DT_US[15:8]							
4A2	1186	IMEM_SRAM_APEX_REG_1186	R/W	GAF_CONFIG_GYR_DT_US[23:16]							
4A3	1187	IMEM_SRAM_APEX_REG_1187	R/W	GAF_CONFIG_GYR_DT_US[31:24]							
4A8	1192	IMEM_SRAM_APEX_REG_1192	R/W	GAF_CONFIG_MAG_DT_US[7:0]							
4A9	1193	IMEM_SRAM_APEX_REG_1193	R/W	GAF_CONFIG_MAG_DT_US[15:8]							
4AA	1194	IMEM_SRAM_APEX_REG_1194	R/W	GAF_CONFIG_MAG_DT_US[23:16]							
4AB	1195	IMEM_SRAM_APEX_REG_1195	R/W	GAF_CONFIG_MAG_DT_US[31:24]							
4B8	1208	IMEM_SRAM_APEX_REG_1208	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[7:0]							
4B9	1209	IMEM_SRAM_APEX_REG_1209	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[15:8]							
4BA	1210	IMEM_SRAM_APEX_REG_1210	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[23:16]							
4BB	1211	IMEM_SRAM_APEX_REG_1211	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[31:24]							
4BC	1212	IMEM_SRAM_APEX_REG_1212	R/W	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[7:0]							
4BD	1213	IMEM_SRAM_APEX_REG_1213	R/W	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[15:8]							
4BE	1214	IMEM_SRAM_APEX_REG_1214	R/W	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[23:16]							
4BF	1215	IMEM_SRAM_APEX_REG_1215	R/W	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[31:24]							
4C4	1220	IMEM_SRAM_APEX_REG_1220	R/W	GAF_CONFIG_MAG_THR_LOCK_ACC[7:0]							
4C5	1221	IMEM_SRAM_APEX_REG_1221	R/W	GAF_CONFIG_MAG_THR_LOCK_ACC[15:8]							
4C6	1222	IMEM_SRAM_APEX_REG_1222	R/W	GAF_CONFIG_MAG_THR_LOCK_ACC[23:16]							
4C7	1223	IMEM_SRAM_APEX_REG_1223	R/W	GAF_CONFIG_MAG_THR_LOCK_ACC[31:24]							
4D0	1232	IMEM_SRAM_APEX_REG_1232	R/W	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[7:0]							
4D1	1233	IMEM_SRAM_APEX_REG_1233	R/W	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[15:8]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
4D2	1234	IMEM_SRAM_APEX_REG_1234	R/W	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[23:16]							
4D3	1235	IMEM_SRAM_APEX_REG_1235	R/W	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[31:24]							
4D4	1236	IMEM_SRAM_APEX_REG_1236	R/W	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[7:0]							
4D5	1237	IMEM_SRAM_APEX_REG_1237	R/W	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[15:8]							
4D6	1238	IMEM_SRAM_APEX_REG_1238	R/W	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[23:16]							
4D7	1239	IMEM_SRAM_APEX_REG_1239	R/W	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[31:24]							
4D8	1240	IMEM_SRAM_APEX_REG_1240	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[7:0]							
4D9	1241	IMEM_SRAM_APEX_REG_1241	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[15:8]							
4DA	1242	IMEM_SRAM_APEX_REG_1242	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[23:16]							
4DB	1243	IMEM_SRAM_APEX_REG_1243	R/W	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[31:24]							
4F4	1268	IMEM_SRAM_APEX_REG_1268	R/W	GAF_CONFIG_FUS_ACCELERATION_REJECTION[7:0]							
4F5	1269	IMEM_SRAM_APEX_REG_1269	R/W	GAF_CONFIG_FUS_ACCELERATION_REJECTION[15:8]							
4F6	1270	IMEM_SRAM_APEX_REG_1270	R/W	GAF_CONFIG_FUS_ACCELERATION_REJECTION[23:16]							
4F7	1271	IMEM_SRAM_APEX_REG_1271	R/W	GAF_CONFIG_FUS_ACCELERATION_REJECTION[31:24]							
4F8	1272	IMEM_SRAM_APEX_REG_1272	R/W	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[7:0]							
4F9	1273	IMEM_SRAM_APEX_REG_1273	R/W	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[15:8]							
4FA	1274	IMEM_SRAM_APEX_REG_1274	R/W	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[23:16]							
4FB	1275	IMEM_SRAM_APEX_REG_1275	R/W	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[31:24]							
5BC	1468	IMEM_SRAM_APEX_REG_1468	R/W	GAF_SAVED_GYR_ACCURACY[7:0]							
5BD	1469	IMEM_SRAM_APEX_REG_1469	R/W	GAF_SAVED_GYR_ACCURACY[15:8]							
5BE	1470	IMEM_SRAM_APEX_REG_1470	R/W	GAF_SAVED_GYR_ACCURACY[23:16]							
5BF	1471	IMEM_SRAM_APEX_REG_1471	R/W	GAF_SAVED_GYR_ACCURACY[31:24]							
5CC	1484	IMEM_SRAM_APEX_REG_1484	R/W	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[7:0]							
5CD	1485	IMEM_SRAM_APEX_REG_1485	R/W	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[15:8]							
5CE	1486	IMEM_SRAM_APEX_REG_1486	R/W	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[23:16]							
5CF	1487	IMEM_SRAM_APEX_REG_1487	R/W	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[31:24]							
5DC	1500	IMEM_SRAM_APEX_REG_1500	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[7:0]							
5DD	1501	IMEM_SRAM_APEX_REG_1501	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[15:8]							
5DE	1502	IMEM_SRAM_APEX_REG_1502	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[23:16]							
5DF	1503	IMEM_SRAM_APEX_REG_1503	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[31:24]							
5E0	1504	IMEM_SRAM_APEX_REG_1504	R/W	GAF_CONFIG_GYR_BIAS_REJECT_TH[7:0]							
5E1	1505	IMEM_SRAM_APEX_REG_1505	R/W	GAF_CONFIG_GYR_BIAS_REJECT_TH[15:8]							
5E2	1506	IMEM_SRAM_APEX_REG_1506	R/W	GAF_CONFIG_GYR_BIAS_REJECT_TH[23:16]							
5E3	1507	IMEM_SRAM_APEX_REG_1507	R/W	GAF_CONFIG_GYR_BIAS_REJECT_TH[31:24]							
5EC	1516	IMEM_SRAM_APEX_REG_1516	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[7:0]							
5ED	1517	IMEM_SRAM_APEX_REG_1517	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[15:8]							
5EE	1518	IMEM_SRAM_APEX_REG_1518	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[23:16]							
5EF	1519	IMEM_SRAM_APEX_REG_1519	R/W	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[31:24]							
6A0	1696	IMEM_SRAM_APEX_REG_1696	R/W	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[7:0]							
6A1	1697	IMEM_SRAM_APEX_REG_1697	R/W	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[15:8]							
6A2	1698	IMEM_SRAM_APEX_REG_1698	R/W	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[23:16]							
6A3	1699	IMEM_SRAM_APEX_REG_1699	R/W	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[31:24]							
6B0	1712	IMEM_SRAM_APEX_REG_1712	R/W	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[7:0]							
6B1	1713	IMEM_SRAM_APEX_REG_1713	R/W	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[15:8]							
6B2	1714	IMEM_SRAM_APEX_REG_1714	R/W	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[23:16]							
6B3	1715	IMEM_SRAM_APEX_REG_1715	R/W	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[31:24]							
6B4	1716	IMEM_SRAM_APEX_REG_1716	R/W	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[7:0]							
6B5	1717	IMEM_SRAM_APEX_REG_1717	R/W	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[15:8]							
6B6	1718	IMEM_SRAM_APEX_REG_1718	R/W	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[23:16]							
6B7	1719	IMEM_SRAM_APEX_REG_1719	R/W	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[31:24]							
6B8	1720	IMEM_SRAM_APEX_REG_1720	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[7:0]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6B9	1721	IMEM_SRAM_APEX_REG_1721	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[15:8]							
6BA	1722	IMEM_SRAM_APEX_REG_1722	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[23:16]							
6BB	1723	IMEM_SRAM_APEX_REG_1723	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[31:24]							
6BC	1724	IMEM_SRAM_APEX_REG_1724	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[7:0]							
6BD	1725	IMEM_SRAM_APEX_REG_1725	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[15:8]							
6BE	1726	IMEM_SRAM_APEX_REG_1726	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[23:16]							
6BF	1727	IMEM_SRAM_APEX_REG_1727	R/W	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[31:24]							
6C0	1728	IMEM_SRAM_APEX_REG_1728	R/W	GAF_CONFIG_GOLDEN_BIAS_TIMER[7:0]							
6C1	1729	IMEM_SRAM_APEX_REG_1729	R/W	GAF_CONFIG_GOLDEN_BIAS_TIMER[15:8]							
6C2	1730	IMEM_SRAM_APEX_REG_1730	R/W	GAF_CONFIG_GOLDEN_BIAS_TIMER[23:16]							
6C3	1731	IMEM_SRAM_APEX_REG_1731	R/W	GAF_CONFIG_GOLDEN_BIAS_TIMER[31:24]							
6C4	1732	IMEM_SRAM_APEX_REG_1732	R/W	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[7:0]							
6C5	1733	IMEM_SRAM_APEX_REG_1733	R/W	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[15:8]							
6C6	1734	IMEM_SRAM_APEX_REG_1734	R/W	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[23:16]							
6C7	1735	IMEM_SRAM_APEX_REG_1735	R/W	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[31:24]							
6C8	1736	IMEM_SRAM_APEX_REG_1736	R/W	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[7:0]							
6C9	1737	IMEM_SRAM_APEX_REG_1737	R/W	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[15:8]							
6CA	1738	IMEM_SRAM_APEX_REG_1738	R/W	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[23:16]							
6CB	1739	IMEM_SRAM_APEX_REG_1739	R/W	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[31:24]							
6CC	1740	IMEM_SRAM_APEX_REG_1740	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[7:0]							
6CD	1741	IMEM_SRAM_APEX_REG_1741	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[15:8]							
6CE	1742	IMEM_SRAM_APEX_REG_1742	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[23:16]							
6CF	1743	IMEM_SRAM_APEX_REG_1743	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[31:24]							
6D0	1744	IMEM_SRAM_APEX_REG_1744	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[39:32]							
6D1	1745	IMEM_SRAM_APEX_REG_1745	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[47:40]							
6D2	1746	IMEM_SRAM_APEX_REG_1746	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[55:48]							
6D3	1747	IMEM_SRAM_APEX_REG_1747	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[63:56]							
6D4	1748	IMEM_SRAM_APEX_REG_1748	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[71:64]							
6D5	1749	IMEM_SRAM_APEX_REG_1749	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[79:72]							
6D6	1750	IMEM_SRAM_APEX_REG_1750	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[87:80]							
6D7	1751	IMEM_SRAM_APEX_REG_1751	R/W	GAF_SAVED_GYR_BIAS_DPS_Q12[95:88]							
76C	1900	IMEM_SRAM_APEX_REG_1900	R/W	GAF_SAVED_MAG_ACCURACY_COVARIANCE[7:0]							
76D	1901	IMEM_SRAM_APEX_REG_1901	R/W	GAF_SAVED_MAG_ACCURACY_COVARIANCE[15:8]							
76E	1902	IMEM_SRAM_APEX_REG_1902	R/W	GAF_SAVED_MAG_ACCURACY_COVARIANCE[23:16]							
76F	1903	IMEM_SRAM_APEX_REG_1903	R/W	GAF_SAVED_MAG_ACCURACY_COVARIANCE[31:24]							
770	1904	IMEM_SRAM_APEX_REG_1904	R/W	GAF_SAVED_MAG_ACCURACY[7:0]							
771	1905	IMEM_SRAM_APEX_REG_1905	R/W	GAF_SAVED_MAG_ACCURACY[15:8]							
772	1906	IMEM_SRAM_APEX_REG_1906	R/W	GAF_SAVED_MAG_ACCURACY[23:16]							
773	1907	IMEM_SRAM_APEX_REG_1907	R/W	GAF_SAVED_MAG_ACCURACY[31:24]							
774	1908	IMEM_SRAM_APEX_REG_1908	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[7:0]							
775	1909	IMEM_SRAM_APEX_REG_1909	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[15:8]							
776	1910	IMEM_SRAM_APEX_REG_1910	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[23:16]							
777	1911	IMEM_SRAM_APEX_REG_1911	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[31:24]							
778	1912	IMEM_SRAM_APEX_REG_1912	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[39:32]							
779	1913	IMEM_SRAM_APEX_REG_1913	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[47:40]							
77A	1914	IMEM_SRAM_APEX_REG_1914	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[55:48]							
77B	1915	IMEM_SRAM_APEX_REG_1915	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[63:56]							
77C	1916	IMEM_SRAM_APEX_REG_1916	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[71:64]							
77D	1917	IMEM_SRAM_APEX_REG_1917	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[79:72]							
77E	1918	IMEM_SRAM_APEX_REG_1918	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[87:80]							
77F	1919	IMEM_SRAM_APEX_REG_1919	R/W	GAF_SAVED_MAG_BIAS_UT_Q16[95:88]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
818	2072	IMEM_SRAM_APEX_REG_2072	R/W	GAF_CONFIG_MAGCAL_DT_US[7:0]							
819	2073	IMEM_SRAM_APEX_REG_2073	R/W	GAF_CONFIG_MAGCAL_DT_US[15:8]							
81A	2074	IMEM_SRAM_APEX_REG_2074	R/W	GAF_CONFIG_MAGCAL_DT_US[23:16]							
81B	2075	IMEM_SRAM_APEX_REG_2075	R/W	GAF_CONFIG_MAGCAL_DT_US[31:24]							
820	2080	IMEM_SRAM_APEX_REG_2080	R/W	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[7:0]							
821	2081	IMEM_SRAM_APEX_REG_2081	R/W	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[15:8]							
822	2082	IMEM_SRAM_APEX_REG_2082	R/W	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[23:16]							
823	2083	IMEM_SRAM_APEX_REG_2083	R/W	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[31:24]							
824	2084	IMEM_SRAM_APEX_REG_2084	R/W	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[7:0]							
825	2085	IMEM_SRAM_APEX_REG_2085	R/W	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[15:8]							
826	2086	IMEM_SRAM_APEX_REG_2086	R/W	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[23:16]							
827	2087	IMEM_SRAM_APEX_REG_2087	R/W	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[31:24]							
828	2088	IMEM_SRAM_APEX_REG_2088	R/W	GAF_CONFIG_MAG_THR_SELECT_ANGLE[7:0]							
829	2089	IMEM_SRAM_APEX_REG_2089	R/W	GAF_CONFIG_MAG_THR_SELECT_ANGLE[15:8]							
82A	2090	IMEM_SRAM_APEX_REG_2090	R/W	GAF_CONFIG_MAG_THR_SELECT_ANGLE[23:16]							
82B	2091	IMEM_SRAM_APEX_REG_2091	R/W	GAF_CONFIG_MAG_THR_SELECT_ANGLE[31:24]							
82C	2092	IMEM_SRAM_APEX_REG_2092	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[7:0]							
82D	2093	IMEM_SRAM_APEX_REG_2093	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[15:8]							
82E	2094	IMEM_SRAM_APEX_REG_2094	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[23:16]							
82F	2095	IMEM_SRAM_APEX_REG_2095	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[31:24]							
830	2096	IMEM_SRAM_APEX_REG_2096	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[7:0]							
831	2097	IMEM_SRAM_APEX_REG_2097	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[15:8]							
832	2098	IMEM_SRAM_APEX_REG_2098	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[23:16]							
833	2099	IMEM_SRAM_APEX_REG_2099	R/W	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[31:24]							
834	2100	IMEM_SRAM_APEX_REG_2100	R/W	GAF_CONFIG_MAG_Q0_STANDALONE[7:0]							
835	2101	IMEM_SRAM_APEX_REG_2101	R/W	GAF_CONFIG_MAG_Q0_STANDALONE[15:8]							
836	2102	IMEM_SRAM_APEX_REG_2102	R/W	GAF_CONFIG_MAG_Q0_STANDALONE[23:16]							
837	2103	IMEM_SRAM_APEX_REG_2103	R/W	GAF_CONFIG_MAG_Q0_STANDALONE[31:24]							
838	2104	IMEM_SRAM_APEX_REG_2104	R/W	GAF_CONFIG_MAG_R0_STANDALONE[7:0]							
839	2105	IMEM_SRAM_APEX_REG_2105	R/W	GAF_CONFIG_MAG_R0_STANDALONE[15:8]							
83A	2106	IMEM_SRAM_APEX_REG_2106	R/W	GAF_CONFIG_MAG_R0_STANDALONE[23:16]							
83B	2107	IMEM_SRAM_APEX_REG_2107	R/W	GAF_CONFIG_MAG_R0_STANDALONE[31:24]							
83C	2108	IMEM_SRAM_APEX_REG_2108	R/W	GAF_CONFIG_MAG_Q0_ASSISTED[7:0]							
83D	2109	IMEM_SRAM_APEX_REG_2109	R/W	GAF_CONFIG_MAG_Q0_ASSISTED[15:8]							
83E	2110	IMEM_SRAM_APEX_REG_2110	R/W	GAF_CONFIG_MAG_Q0_ASSISTED[23:16]							
83F	2111	IMEM_SRAM_APEX_REG_2111	R/W	GAF_CONFIG_MAG_Q0_ASSISTED[31:24]							
840	2112	IMEM_SRAM_APEX_REG_2112	R/W	GAF_CONFIG_MAG_R0_ASSISTED[7:0]							
841	2113	IMEM_SRAM_APEX_REG_2113	R/W	GAF_CONFIG_MAG_R0_ASSISTED[15:8]							
842	2114	IMEM_SRAM_APEX_REG_2114	R/W	GAF_CONFIG_MAG_R0_ASSISTED[23:16]							
843	2115	IMEM_SRAM_APEX_REG_2115	R/W	GAF_CONFIG_MAG_R0_ASSISTED[31:24]							
844	2116	IMEM_SRAM_APEX_REG_2116	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[7:0]							
845	2117	IMEM_SRAM_APEX_REG_2117	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[15:8]							
846	2118	IMEM_SRAM_APEX_REG_2118	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[23:16]							
847	2119	IMEM_SRAM_APEX_REG_2119	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[31:24]							
848	2120	IMEM_SRAM_APEX_REG_2120	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS[7:0]							
849	2121	IMEM_SRAM_APEX_REG_2121	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS[15:8]							
84A	2122	IMEM_SRAM_APEX_REG_2122	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS[23:16]							
84B	2123	IMEM_SRAM_APEX_REG_2123	R/W	GAF_CONFIG_MAG_THR_MAX_RADIUS[31:24]							
84C	2124	IMEM_SRAM_APEX_REG_2124	R/W	GAF_CONFIG_MAG_THR_MIN_RADIUS[7:0]							
84D	2125	IMEM_SRAM_APEX_REG_2125	R/W	GAF_CONFIG_MAG_THR_MIN_RADIUS[15:8]							
84E	2126	IMEM_SRAM_APEX_REG_2126	R/W	GAF_CONFIG_MAG_THR_MIN_RADIUS[23:16]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
84F	2127	IMEM_SRAM_APEX_REG_2127	R/W	GAF_CONFIG_MAG_THR_MIN_RADIUS[31:24]							
850	2128	IMEM_SRAM_APEX_REG_2128	R/W	GAF_CONFIG_MAG_CALIBRATION_CONDITION[7:0]							
851	2129	IMEM_SRAM_APEX_REG_2129	R/W	GAF_CONFIG_MAG_CALIBRATION_CONDITION[15:8]							
8C8	2248	IMEM_SRAM_APEX_REG_2248	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[7:0]							
8C9	2249	IMEM_SRAM_APEX_REG_2249	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[15:8]							
8CA	2250	IMEM_SRAM_APEX_REG_2250	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[23:16]							
8CB	2251	IMEM_SRAM_APEX_REG_2251	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[31:24]							
8CC	2252	IMEM_SRAM_APEX_REG_2252	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[39:32]							
8CD	2253	IMEM_SRAM_APEX_REG_2253	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[47:40]							
8CE	2254	IMEM_SRAM_APEX_REG_2254	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[55:48]							
8CF	2255	IMEM_SRAM_APEX_REG_2255	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[63:56]							
8D0	2256	IMEM_SRAM_APEX_REG_2256	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[71:64]							
8D1	2257	IMEM_SRAM_APEX_REG_2257	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[79:72]							
8D2	2258	IMEM_SRAM_APEX_REG_2258	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[87:80]							
8D3	2259	IMEM_SRAM_APEX_REG_2259	R/W	GAF_SAVED_ACC_BIAS_1G_Q16[95:88]							
923	2339	IMEM_SRAM_APEX_REG_2339	R/W	GAF_SAVED_ACC_ACCURACY[7:0]							
924	2340	IMEM_SRAM_APEX_REG_2340	R/W	GAF_INIT_STATUS[7:0]							
96C	2412	IMEM_SRAM_APEX_REG_2412	R/W	GAF_READ_GYR_BIAS_DPS_Q12[7:0]							
96D	2413	IMEM_SRAM_APEX_REG_2413	R/W	GAF_READ_GYR_BIAS_DPS_Q12[15:8]							
96E	2414	IMEM_SRAM_APEX_REG_2414	R/W	GAF_READ_GYR_BIAS_DPS_Q12[23:16]							
96F	2415	IMEM_SRAM_APEX_REG_2415	R/W	GAF_READ_GYR_BIAS_DPS_Q12[31:24]							
970	2416	IMEM_SRAM_APEX_REG_2416	R/W	GAF_READ_GYR_BIAS_DPS_Q12[39:32]							
971	2417	IMEM_SRAM_APEX_REG_2417	R/W	GAF_READ_GYR_BIAS_DPS_Q12[47:40]							
974	2420	IMEM_SRAM_APEX_REG_2420	R/W	GAF_READ_MAG_BIAS_UT_Q16[7:0]							
975	2421	IMEM_SRAM_APEX_REG_2421	R/W	GAF_READ_MAG_BIAS_UT_Q16[15:8]							
976	2422	IMEM_SRAM_APEX_REG_2422	R/W	GAF_READ_MAG_BIAS_UT_Q16[23:16]							
977	2423	IMEM_SRAM_APEX_REG_2423	R/W	GAF_READ_MAG_BIAS_UT_Q16[31:24]							
978	2424	IMEM_SRAM_APEX_REG_2424	R/W	GAF_READ_MAG_BIAS_UT_Q16[39:32]							
979	2425	IMEM_SRAM_APEX_REG_2425	R/W	GAF_READ_MAG_BIAS_UT_Q16[47:40]							
97A	2426	IMEM_SRAM_APEX_REG_2426	R/W	GAF_READ_MAG_BIAS_UT_Q16[55:48]							
97B	2427	IMEM_SRAM_APEX_REG_2427	R/W	GAF_READ_MAG_BIAS_UT_Q16[63:56]							
97C	2428	IMEM_SRAM_APEX_REG_2428	R/W	GAF_READ_MAG_BIAS_UT_Q16[71:64]							
97D	2429	IMEM_SRAM_APEX_REG_2429	R/W	GAF_READ_MAG_BIAS_UT_Q16[79:72]							
97E	2430	IMEM_SRAM_APEX_REG_2430	R/W	GAF_READ_MAG_BIAS_UT_Q16[87:80]							
97F	2431	IMEM_SRAM_APEX_REG_2431	R/W	GAF_READ_MAG_BIAS_UT_Q16[95:88]							
981	2433	IMEM_SRAM_APEX_REG_2433	R/W	GAF_READ_MAG_ACCURACY[7:0]							
9DC	2524	IMEM_SRAM_APEX_REG_2524	R/W	SIF_TIME_FEAS_CONFIG[7:0]							
9DD	2525	IMEM_SRAM_APEX_REG_2525	R/W	SIF_TIME_FEAS_CONFIG[15:8]							
9F4	2548	IMEM_SRAM_APEX_REG_2548	R/W	SIF_CLASS_INDEX[7:0]							
9F5	2549	IMEM_SRAM_APEX_REG_2549	R/W	SIF_CLASS_INDEX[15:8]							
A34	2612	IMEM_SRAM_APEX_REG_2612	R/W	SIF_CCONFIG[7:0]							
A35	2613	IMEM_SRAM_APEX_REG_2613	R/W	SIF_CCONFIG[15:8]							
A36	2614	IMEM_SRAM_APEX_REG_2614	R/W	SIF_CCONFIG[23:16]							
A37	2615	IMEM_SRAM_APEX_REG_2615	R/W	SIF_CCONFIG[31:24]							
A38	2616	IMEM_SRAM_APEX_REG_2616	R/W	SIF_CCONFIG[39:32]							
A39	2617	IMEM_SRAM_APEX_REG_2617	R/W	SIF_CCONFIG[47:40]							
A3A	2618	IMEM_SRAM_APEX_REG_2618	R/W	SIF_CCONFIG[55:48]							
A3B	2619	IMEM_SRAM_APEX_REG_2619	R/W	SIF_CCONFIG[63:56]							
A3C	2620	IMEM_SRAM_APEX_REG_2620	R/W	SIF_CCONFIG[71:64]							
A3D	2621	IMEM_SRAM_APEX_REG_2621	R/W	SIF_CCONFIG[79:72]							
A3E	2622	IMEM_SRAM_APEX_REG_2622	R/W	SIF_CCONFIG[87:80]							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A3F	2623	IMEM_SRAM_APEX_REG_2623	R/W	SIF_CCONFIG[95:88]							
A40	2624	IMEM_SRAM_APEX_REG_2624	R/W	SIF_TCONFIG[7:0]							
A41	2625	IMEM_SRAM_APEX_REG_2625	R/W	SIF_TCONFIG[15:8]							
A42	2626	IMEM_SRAM_APEX_REG_2626	R/W	SIF_TCONFIG[23:16]							
A43	2627	IMEM_SRAM_APEX_REG_2627	R/W	SIF_TCONFIG[31:24]							
A44	2628	IMEM_SRAM_APEX_REG_2628	R/W	SIF_TCONFIG[39:32]							
A45	2629	IMEM_SRAM_APEX_REG_2629	R/W	SIF_TCONFIG[47:40]							
A46	2630	IMEM_SRAM_APEX_REG_2630	R/W	SIF_TCONFIG[55:48]							
A47	2631	IMEM_SRAM_APEX_REG_2631	R/W	SIF_TCONFIG[63:56]							
A48	2632	IMEM_SRAM_APEX_REG_2632	R/W	SIF_TCONFIG[71:64]							
A49	2633	IMEM_SRAM_APEX_REG_2633	R/W	SIF_TCONFIG[79:72]							
A4A	2634	IMEM_SRAM_APEX_REG_2634	R/W	SIF_TCONFIG[87:80]							
A4B	2635	IMEM_SRAM_APEX_REG_2635	R/W	SIF_TCONFIG[95:88]							
A4C	2636	IMEM_SRAM_APEX_REG_2636	R/W	SIF_TCONFIG[103:96]							
A4D	2637	IMEM_SRAM_APEX_REG_2637	R/W	SIF_TCONFIG[111:104]							
A4E	2638	IMEM_SRAM_APEX_REG_2638	R/W	SIF_TCONFIG[119:112]							
A4F	2639	IMEM_SRAM_APEX_REG_2639	R/W	SIF_TCONFIG[127:120]							
A50	2640	IMEM_SRAM_APEX_REG_2640	R/W	SIF_TCONFIG[135:128]							
A51	2641	IMEM_SRAM_APEX_REG_2641	R/W	SIF_TCONFIG[143:136]							
A52	2642	IMEM_SRAM_APEX_REG_2642	R/W	SIF_TCONFIG[151:144]							
A53	2643	IMEM_SRAM_APEX_REG_2643	R/W	SIF_TCONFIG[159:152]							
A54	2644	IMEM_SRAM_APEX_REG_2644	R/W	SIF_TCONFIG[167:160]							
A55	2645	IMEM_SRAM_APEX_REG_2645	R/W	SIF_TCONFIG[175:168]							
A56	2646	IMEM_SRAM_APEX_REG_2646	R/W	SIF_TCONFIG[183:176]							
A57	2647	IMEM_SRAM_APEX_REG_2647	R/W	SIF_TCONFIG[191:184]							
A5C to AA7	2652 to 2727	IMEM_SRAM_APEX_REG_2652 to IMEM_SRAM_APEX_REG_2727	R/W	SIF_FILTER[607:0]							
138C	5004	IMEM_SRAM_APEX_REG_5004	R/W	SIF_TREE_THRESHOLDS[7:0]							
138D	5005	IMEM_SRAM_APEX_REG_5005	R/W	SIF_TREE_THRESHOLDS[15:8]							
158A	5514	IMEM_SRAM_APEX_REG_5514	R/W	SIF_TREE_FEATUREIDS[7:0]							
1689	5769	IMEM_SRAM_APEX_REG_5769	R/W	SIF_TREE_NEXTNODERIGHT[7:0]							
1788	6024	IMEM_SRAM_APEX_REG_6024	R/W	SIF_TREE_THRESHOLDSSHIFT[7:0]							

15.4 USER BANK IMEM_SRAM_STC REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
34	52	IMEM_SRAM_STC_REG_52	R/W	STC_CONFIGPARAMS[7:0]							
35	53	IMEM_SRAM_STC_REG_53	R/W	STC_CONFIGPARAMS[15:8]							
36	54	IMEM_SRAM_STC_REG_54	R/W	STC_CONFIGPARAMS[23:16]							
37	55	IMEM_SRAM_STC_REG_55	R/W	STC_CONFIGPARAMS[31:24]							
38	56	IMEM_SRAM_STC_REG_56	R/W	STC_RESULTS[7:0]							
39	57	IMEM_SRAM_STC_REG_57	R/W	STC_RESULTS[15:8]							
3A	58	IMEM_SRAM_STC_REG_58	R/W	STC_RESULTS[23:16]							
3B	59	IMEM_SRAM_STC_REG_59	R/W	STC_RESULTS[31:24]							

15.5 USER BANK IPREG_BAR REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
39	57	IPREG_BAR_REG_57	R/W	-	IO_OPT0	IO_OPT1	-				
3A	58	IPREG_BAR_REG_58	R/W	PADS_AP_SCLK_PUD_TRIM_D2A	PADS_AP_SCLK_PE_TRIM_D2A	-	PADS_AP_CS_PUD_TRIM_D2A	PADS_AP_CS_PE_TRIM_D2A	-		IO_OPT2
3B	59	IPREG_BAR_REG_59	R/W	PADS_PIN7_PE_TRIM_D2A	-	PADS_AP_SDO_PUD_TRIM_D2A	PADS_AP_SDO_PE_TRIM_D2A	-	PADS_AP_SDI_PUD_TRIM_D2A	PADS_AP_SDI_PE_TRIM_D2A	-
3C	60	IPREG_BAR_REG_60	R/W	-	PADS_AUX1_SCLK_PUD_TRIM_D2A	PADS_AUX1_SCLK_PE_TRIM_D2A	PADS_AUX_SCLK_TP2_FROM_PAD_DISABLE_TRIM_D2A	PADS_AUX1_CS_PUD_TRIM_D2A	PADS_AUX1_CS_PE_TRIM_D2A	-	PADS_PIN7_CS_PUD_TRIM_D2A
3D	61	IPREG_BAR_REG_61	R/W	PADS_INT1_PUD_TRIM_D2A	PADS_INT1_PE_TRIM_D2A	-	PADS_AUX1_SDO_PUD_TRIM_D2A	PADS_AUX1_SDO_PE_TRIM_D2A	-	PADS_AUX1_SDI_PUD_TRIM_D2A	PADS_AUX1_SDI_PE_TRIM_D2A
3E	62	IPREG_BAR_REG_62	R/W	-					PADS_INT2_PUD_TRIM_D2A	PADS_INT2_PE_TRIM_D2A	-

15.6 USER BANK IPREG_TOP1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
06	06	I2CM_COMMAND_0	R/W	ENDFLAG_0	CH_SEL_0	R_W_0		BURSTLEN_0			
07	07	I2CM_COMMAND_1	R/W	ENDFLAG_1	CH_SEL_1	R_W_1		BURSTLEN_1			
08	08	I2CM_COMMAND_2	R/W	ENDFLAG_2	CH_SEL_2	R_W_2		BURSTLEN_2			
09	09	I2CM_COMMAND_3	R/W	ENDFLAG_3	CH_SEL_3	R_W_3		BURSTLEN_3			
0E	14	I2CM_DEV_PROFILE0	R/W	RD_ADDRESS_0							
0F	15	I2CM_DEV_PROFILE1	R/W	-	DEV_ID_0						
10	16	I2CM_DEV_PROFILE2	R/W	RD_ADDRESS_1							
11	17	I2CM_DEV_PROFILE3	R/W	-	DEV_ID_1						
16	22	I2CM_CONTROL	RWS	-	I2CM_RESTART_EN	-		I2CM_SPEED	-		I2CM_GO
18	24	I2CM_STATUS	R	-		I2CM_SDA_ERR	I2CM_SCL_ERR	I2CM_SRST_ERR	I2CM_TIMEOUT_ERR	I2CM_DONE	I2CM_BUSY
1A	26	I2CM_EXT_DEV_STATUS		-				I2CM_EXT_DEV_STATUS			
1B	27	I2CM_RD_DATA0	RWS	I2CM_RD_DATA0							
1C	28	I2CM_RD_DATA1	RWS	I2CM_RD_DATA1							
1D	29	I2CM_RD_DATA2	RWS	I2CM_RD_DATA2							
1E	30	I2CM_RD_DATA3	RWS	I2CM_RD_DATA3							
1F	31	I2CM_RD_DATA4	RWS	I2CM_RD_DATA4							
20	32	I2CM_RD_DATA5	RWS	I2CM_RD_DATA5							
21	33	I2CM_RD_DATA6	RWS	I2CM_RD_DATA6							
22	34	I2CM_RD_DATA7	RWS	I2CM_RD_DATA7							
23	35	I2CM_RD_DATA8	RWS	I2CM_RD_DATA8							
24	36	I2CM_RD_DATA9	RWS	I2CM_RD_DATA9							
25	37	I2CM_RD_DATA10	RWS	I2CM_RD_DATA10							
26	38	I2CM_RD_DATA11	RWS	I2CM_RD_DATA11							
27	39	I2CM_RD_DATA12	RWS	I2CM_RD_DATA12							
28	40	I2CM_RD_DATA13	RWS	I2CM_RD_DATA13							
29	41	I2CM_RD_DATA14	RWS	I2CM_RD_DATA14							
2A	42	I2CM_RD_DATA15	RWS	I2CM_RD_DATA15							
2B	43	I2CM_RD_DATA16	RWS	I2CM_RD_DATA16							
2C	44	I2CM_RD_DATA17	RWS	I2CM_RD_DATA17							
2D	45	I2CM_RD_DATA18	RWS	I2CM_RD_DATA18							

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2E	46	I2CM_RD_DATA19	RWS	I2CM_RD_DATA19							
2F	47	I2CM_RD_DATA20	RWS	I2CM_RD_DATA20							
33	51	I2CM_WR_DATA0	R/W	I2CM_WR_DATA0							
34	52	I2CM_WR_DATA1	R/W	I2CM_WR_DATA1							
35	53	I2CM_WR_DATA2	R/W	I2CM_WR_DATA2							
36	54	I2CM_WR_DATA3	R/W	I2CM_WR_DATA3							
37	55	I2CM_WR_DATA4	R/W	I2CM_WR_DATA4							
38	56	I2CM_WR_DATA5	R/W	I2CM_WR_DATA5							
4B	75	SIFS_IXC_ERROR_STATUS	R/C	-						AUX1_SIFS_IXC_TIMEOUT_ERR	SIFS_IXC_TIMEOUT_ERR
4F	79	EDMP_PRGRM_IRQ0_0	R/W	PRGRM_STRT_ADDR_IRQ_0[7:0]							
50	80	EDMP_PRGRM_IRQ0_1	R/W	PRGRM_STRT_ADDR_IRQ_0[15:8]							
51	81	EDMP_PRGRM_IRQ1_0	R/W	PRGRM_STRT_ADDR_IRQ_1[7:0]							
52	82	EDMP_PRGRM_IRQ1_1	R/W	PRGRM_STRT_ADDR_IRQ_1[15:8]							
53	83	EDMP_PRGRM_IRQ2_0	R/W	PRGRM_STRT_ADDR_IRQ_2[7:0]							
54	84	EDMP_PRGRM_IRQ2_1	R/W	PRGRM_STRT_ADDR_IRQ_2[15:8]							
55	85	EDMP_SP_START_ADDR	R/W	EDMP_SP_START_ADDR							
58	88	SMC_CONTROL_0	R/W	-			ACCEL_LP_CLK_SEL	TEMP_DIS	TMST_FORCE_AUX_FINE_EN	TMST_FSYNC_EN	TMST_EN
59	89	SMC_CONTROL_1	R/W	-				SREG_AUX_ACCEL_ONLY_EN	-		
63	99	STC_CONFIG	R/W	-				STC_SENSOR_SEL		-	
67	103	SREG_CTRL	R/W	-						SREG_DATA_ENDIAN_SEL	-
68	104	SIFS_I3C_STC_CFG	R/W	-					I3C_STC_MODE	-	
69	105	INT_PULSE_MIN_ON_INTF0	R/W	-					INT0_TPULSE_DURATION		
6A	106	INT_PULSE_MIN_ON_INTF1	R/W	-					INT1_TPULSE_DURATION		
6B	107	INT_PULSE_MIN_OFF_INTF0	R/W	-					INT0_TDEASSERT_DISABLE		
6C	108	INT_PULSE_MIN_OFF_INTF1	R/W	-					INT1_TDEASSERT_DISABLE		
6E	110	ISR_0_7	R/C	-		INT_STATUS_ON_DEMAND_PIN_0	-	INT_STATUS_EXT_ODR_DRDY_PIN_0	-		INT_STATUS_ACCEL_DRDY_PIN_0
6F	111	ISR_8_15	R/C	-		INT_STATUS_ON_DEMAND_PIN_1	-	INT_STATUS_EXT_ODR_DRDY_PIN_1	-		INT_STATUS_ACCEL_DRDY_PIN_1
70	112	ISR_16_23	R/C	-		INT_STATUS_ON_DEMAND_PIN_2	-	INT_STATUS_EXT_ODR_DRDY_PIN_2	-		INT_STATUS_ACCEL_DRDY_PIN_2
71	113	STATUS_MASK_PIN_0_7	R/W	-		INT_ON_DEMAND_PIN_0_DIS	-	INT_EXT_ODR_DRDY_PIN_0_DIS	-		INT_ACCEL_DRDY_PIN_0_DIS
72	114	STATUS_MASK_PIN_8_15	R/W	-		INT_ON_DEMAND_PIN_1_DIS	-	INT_EXT_ODR_DRDY_PIN_1_DIS	-		INT_ACCEL_DRDY_PIN_1_DIS
73	115	STATUS_MASK_PIN_16_23	R/W	-		INT_ON_DEMAND_PIN_2_DIS	-	INT_EXT_ODR_DRDY_PIN_2_DIS	-		INT_ACCEL_DRDY_PIN_2_DIS
74	116	INT_I2CM_SOURCE	R/W	-						INT_STATUS_I2CM_SMC_EXT_ODR_EN	-
7E	126	ACCEL_WOM_X_THR	R/W	WOM_X_TH							
7F	127	ACCEL_WOM_Y_THR	R/W	WOM_Y_TH							
80	128	ACCEL_WOM_Z_THR	R/W	WOM_Z_TH							
90	144	SELFTEST		-		EN_GZ_ST	EN_GY_ST	EN_GX_ST	EN_AZ_ST	EN_AY_ST	EN_AX_ST
97	151	IPREG_MISC	R	-						EDMP_IDLE	-
A2	162	SW_PLL1_TRIM	R	SW_PLL1_TRIM							

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Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
A7	167	FIFO_SRAM_SLEEP	R/W	-						FIFO_GSLEEP_SHARED_SRAM	

15.7 USER BANK IPREG_SYS1 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
2A	42	IPREG_SYS1_REG_42	R/W	GYRO_X_OFFUSER[7:0]							
2B	43	IPREG_SYS1_REG_43	R/W	-		GYRO_X_OFFUSER[13:8]					
38	56	IPREG_SYS1_REG_56	R/W	GYRO_Y_OFFUSER[7:0]							
39	57	IPREG_SYS1_REG_57	R/W	-		GYRO_Y_OFFUSER[13:8]					
46	70	IPREG_SYS1_REG_56	R/W	GYRO_Z_OFFUSER[7:0]							
47	71	IPREG_SYS1_REG_57	R/W	-		GYRO_Z_OFFUSER[13:8]					
A6	166	IPREG_SYS1_REG_166	R/W	-	GYRO_SRC_CTRL		-				
AA	170	IPREG_SYS1_REG_170	R/W	-			GYRO_LP_AVG_SEL				-
AC	172	IPREG_SYS1_REG_172	R/W	-			GYRO_LPF_BYP	-	GYRO_UI_LPFBW_SEL		

15.8 USER BANK IPREG_SYS2 REGISTER MAP

Addr (Hex)	Addr (Dec.)	Register Name	Serial I/F	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
18	24	IPREG_SYS2_REG_24	R/W	ACCEL_X_OFFUSER[7:0]							
19	25	IPREG_SYS2_REG_25	R/W	-		ACCEL_X_OFFUSER[13:8]					
20	32	IPREG_SYS2_REG_32	R/W	ACCEL_Y_OFFUSER[7:0]							
21	33	IPREG_SYS2_REG_33	R/W	-		ACCEL_Y_OFFUSER[13:8]					
28	40	IPREG_SYS2_REG_40	R/W	ACCEL_Z_OFFUSER[7:0]							
29	41	IPREG_SYS2_REG_41	R/W	-		ACCEL_Z_OFFUSER[13:8]					
7B	123	IPREG_SYS2_REG_123	R/W	-						ACCEL_SRC_CTRL	
80	128	IPREG_SYS2_REG_128	R/W	-		TMP_DEC_CFG			TMP_LPF_CFG		
81	129	IPREG_SYS2_REG_129	R/W	-				ACCEL_LP_AVG_SEL			
83	131	IPREG_SYS2_REG_131	R/W	-		ACCEL_LPF_BYP	-		ACCEL_UI_LPFBW_SEL		

Detailed register descriptions are provided in the sections that follow.

Register fields marked as Reserved must not be modified by the user. The Reset Value of the register can be used to determine the default value of reserved register fields, and unless otherwise noted this default value must be maintained even if the values of other register fields are modified by the user.

In the sections that follow, some register fields are described as “can be changed on-the-fly.” These are the only register fields that can be changed on-the-fly even if sensor is on. Register fields not described as such must not be changed on-the-fly if sensor is on.

16 USER BANK 0 REGISTER MAP – DESCRIPTIONS

Please refer to the procedure in Section 14 for configuring device data endianness before using the register map.

16.1 ACCEL_DATA_X1_UI

Name: ACCEL_DATA_X1_UI
Address: 00 (00h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X_UI[15:8]	Upper byte of Accel X-axis data for UI path

16.2 ACCEL_DATA_X0_UI

Name: ACCEL_DATA_X0_UI
Address: 01 (01h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_X_UI[7:0]	Lower byte of Accel X-axis data for UI path

16.3 ACCEL_DATA_Y1_UI

Name: ACCEL_DATA_Y1_UI
Address: 02 (02h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y_UI[15:8]	Upper byte of Accel Y-axis data for UI path

16.4 ACCEL_DATA_Y0_UI

Name: ACCEL_DATA_Y0_UI
Address: 03 (03h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Y_UI[7:0]	Lower byte of Accel Y-axis data for UI path

16.5 ACCEL_DATA_Z1_UI

Name: ACCEL_DATA_Z1_UI
Address: 04 (04h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z_UI[15:8]	Upper byte of Accel Z-axis data for UI path

16.6 ACCEL_DATA_Z0_UI

Name: ACCEL_DATA_Z0_UI
Address: 05 (05h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	ACCEL_DATA_Z_UI[7:0]	Lower byte of Accel Z-axis data for UI path

16.7 GYRO_DATA_X1_UI

Name: GYRO_DATA_X1_UI
Address: 06 (06h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_X_UI[15:8]	Upper byte of Gyro X-axis data for UI path

16.8 GYRO_DATA_X0_UI

Name: GYRO_DATA_X0_UI
Address: 07 (07h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_X_UI[7:0]	Lower byte of Gyro X-axis data for UI path

16.9 GYRO_DATA_Y1_UI

Name: GYRO_DATA_Y1_UI
Address: 08 (08h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y_UI[15:8]	Upper byte of Gyro Y-axis data for UI path

16.10 GYRO_DATA_Y0_UI

Name: GYRO_DATA_Y0_UI
Address: 09 (09h)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Y_UI[7:0]	Lower byte of Gyro Y-axis data for UI path

16.11 GYRO_DATA_Z1_UI

Name: GYRO_DATA_Z1_UI
Address: 10 (0Ah)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z_UI[15:8]	Upper byte of Gyro Z-axis data for UI path

16.12 GYRO_DATA_Z0_UI

Name: GYRO_DATA_Z0_UI
Address: 11 (0Bh)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	GYRO_DATA_Z_UI[7:0]	Lower byte of Gyro Z-axis data for UI path

16.13 TEMP_DATA1_UI

Name: TEMP_DATA1_UI
Address: 12 (0Ch)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	TEMP_DATA_UI[15:8]	Upper byte of temperature data for UI path

16.14 TEMP_DATA0_UI

Name: TEMP_DATA0_UI
Address: 13 (0Dh)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	TEMP_DATA_UI[7:0]	Lower byte of temperature data for UI path

Temperature data value from the sensor data registers can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (TEMP_DATA / 128) + 25

Temperature data stored in FIFO is an 8-bit quantity, FIFO_TEMP_DATA. It can be converted to degrees centigrade by using the following formula:

Temperature in Degrees Centigrade = (FIFO_TEMP_DATA / 2) + 25

16.15 TMST_FSYNCH

Name: TMST_FSYNCH
Address: 14 (0Eh)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[15:8]	Stores the upper byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

16.16 TMST_FSYNCL

Name: TMST_FSYNCL
Address: 15 (0Fh)
Serial IF: SYNCR
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	TMST_FSYNC_DATA_UI[7:0]	Stores the lower byte of the time delta from the rising edge of FSYNC to the latest ODR until the UI Interface reads the FSYNC tag in the status register

16.17 PWR_MGMT0

Name: PWR_MGMT0
Address: 16 (10h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:2	GYRO_MODE	00: Turns gyroscope off 01: Places gyroscope in Standby Mode 10: Places gyroscope in Low Power (LP) Mode 11: Places gyroscope in Low Noise (LN) Mode Can be changed on-the-fly.
1:0	ACCEL_MODE	00: Turns accelerometer off 01: Turns accelerometer off 10: Places accelerometer in Low Power (LP) Mode 11: Places accelerometer in Low Noise (LN) Mode Can be changed on-the-fly.

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16.18 FIFO_COUNT_0

Name: FIFO_COUNT_0
Address: 18 (12h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	FIFO_DATA_CNT[15:8]	High Bits, count indicates the number of packets available in FIFO.

16.19 FIFO_COUNT_1

Name: FIFO_COUNT_1
Address: 19 (13h)
Serial IF: R
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	FIFO_DATA_CNT[7:0]	Low Bits, count indicates the number of packets available in FIFO.

16.20 FIFO_DATA

Name: FIFO_DATA
Address: 20 (14h)
Serial IF: R
Reset value: 0x7F
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	FIFO_DATA	FIFO data port

16.21 INT1_CONFIG0

Name: INT1_CONFIG0
Address: 22 (16h)
Serial IF: R/W
Reset value: 0x80
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT1_STATUS_EN_RESET_DONE	Enable interrupt status bit to flag the occurrence of Reset Done event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
6	INT1_STATUS_EN_AUX1_AGC_RDY	Enable interrupt status bit to flag the occurrence of AUX1 AGC Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
5	INT1_STATUS_EN_AP_AGC_RDY	Enable interrupt status bit to flag the occurrence of UI AGC Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
4	INT1_STATUS_EN_AP_FSYNC	Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
3	INT1_STATUS_EN_AUX1_DRDY	Enable interrupt status bit to flag the occurrence of AUX1 Data Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
2	INT1_STATUS_EN_DRDY	Enable interrupt status bit to flag the occurrence of UI Data Ready event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
1	INT1_STATUS_EN_FIFO_THS	Enable interrupt status bit to flag the occurrence of FIFO count ≥ FIFO threshold event on INT1

		0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
0	INT1_STATUS_EN_FIFO_FULL	Enable interrupt status bit to flag the occurrence of FIFO full event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.

16.22 INT1_CONFIG1

Name: INT1_CONFIG1
Address: 23 (17h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT1_STATUS_EN_APEX_EVENT	Enable interrupt status bit to flag the occurrence of APEX event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
5	INT1_STATUS_EN_I2CM_DONE	Enable interrupt status bit to flag the completion of I^2C master event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
4	INT1_STATUS_EN_I3C_PROTOCOL_ERR	Enable interrupt status bit to flag the occurrence of I3C Protocol Error event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
3	INT1_STATUS_EN_WOM_Z	Enable interrupt status bit to flag the occurrence of WOM on Z-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
2	INT1_STATUS_EN_WOM_Y	Enable interrupt status bit to flag the occurrence of WOM on Y-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
1	INT1_STATUS_EN_WOM_X	Enable interrupt status bit to flag the occurrence of WOM on X-axis event on INT1 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
0	INT1_STATUS_EN_PLL_RDY	Enable interrupt status bit to flag the occurrence of PLL Ready event on INT1 0: Disable interrupt.

		1: Enable interrupt. Setting can be changed by UI interface.

16.23 INT1_CONFIG2

Name: INT1_CONFIG2
Address: 24 (18h)
Serial IF: R/W
Reset value: 0x04
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2	INT1_DRIVE	Sets INT1 to open-drain or push-pull 0: Push-pull 1: Open-drain
1	INT1_MODE	INT1 interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled
0	INT1_POLARITY	INT1 interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled

16.24 INT1_STATUS0

Name: INT1_STATUS0
Address: 25 (19h)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT1_STATUS_RESET_DONE	Flags the occurrence of Reset Done event on INT1 0: Interrupt did not occur 1: Interrupt occurred
6	INT1_STATUS_AUX1_AGC_RDY	Flags the occurrence of AUX1 AGC Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred
5	INT1_STATUS_AP_AGC_RDY	Flags the occurrence of UI AGC Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred
4	INT1_STATUS_AP_FSYNC	Flags the occurrence of UI FSYNC event on INT1 0: Interrupt did not occur 1: Interrupt occurred
3	INT1_STATUS_AUX1_DRDY	Flags the occurrence of AUX1 Data Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred
2	INT1_STATUS_DRDY	Flags the occurrence of UI Data Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred
1	INT1_STATUS_FIFO_THS	Flags the occurrence of FIFO count ≥ FIFO threshold event on INT1 0: Interrupt did not occur 1: Interrupt occurred
0	INT1_STATUS_FIFO_FULL	Flags the occurrence of FIFO full event on INT1 0: Interrupt did not occur 1: Interrupt occurred

16.25 INT1_STATUS1

Name: INT1_STATUS1
Address: 26 (1Ah)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT1_STATUS_APEX_EVENT	Flags the occurrence of APEX event on INT1 0: Interrupt did not occur 1: Interrupt occurred
5	INT1_STATUS_I2CM_DONE	Flags the occurrence of I^2C Master Done event on INT1 0: Interrupt did not occur 1: Interrupt occurred
4	INT1_STATUS_I3C_PROTOCOL_ERR	Flags the occurrence of $I3C^{SM}$ Protocol Error event on INT1 0: Interrupt did not occur 1: Interrupt occurred
3	INT1_STATUS_WOM_Z	Flags the occurrence of Z-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred
2	INT1_STATUS_WOM_Y	Flags the occurrence of Y-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred
1	INT1_STATUS_WOM_X	Flags the occurrence of X-axis WOM event on INT1 0: Interrupt did not occur 1: Interrupt occurred
0	INT1_STATUS_PLL_RDY	Flags the occurrence of PLL Ready event on INT1 0: Interrupt did not occur 1: Interrupt occurred

16.26 ACCEL_CONFIG0

Name: ACCEL_CONFIG0
Address: 27 (1Bh)
Serial IF: R/W
Reset value: 0x06
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6:4	ACCEL_UI_FS_SEL	Full scale select for accelerometer UI interface output 000: Reserved 001: ±16g 010: ±8g 011: ±4g 100: ±2g 101: Reserved 110: Reserved 111: Reserved Can be changed on-the-fly.
3:0	ACCEL_ODR	Accelerometer ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: 6.4kHz (LN mode) 0100: 3.2kHz (LN mode) 0101: 1.6kHz (LN mode) 0110: 800Hz (LN mode) 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode) Can be changed on-the-fly.

16.27 GYRO_CONFIG0

Name: GYRO_CONFIG0
Address: 28 (1Ch)
Serial IF: R/W
Reset value: 0x06
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	GYRO_UI_FS_SEL	Full scale select for gyroscope UI interface output 0000: Reserved 0001: ±2000dps 0010: ±1000dps 0011: ±500dps 0100: ±250dps 0101: ±125dps 0110: ±62.5dps 0111: ±31.25dps 1000: ±15.625dps Rest of the settings are reserved Can be changed on-the-fly.
3:0	GYRO_ODR	Gyroscope ODR selection for UI interface output 0000: Reserved 0001: Reserved 0010: Reserved 0011: 6.4kHz (LN mode) 0100: 3.2kHz (LN mode) 0101: 1.6kHz (LN mode) 0110: 800Hz (LN mode) 0111: 400Hz (LP or LN mode) 1000: 200Hz (LP or LN mode) 1001: 100Hz (LP or LN mode) 1010: 50Hz (LP or LN mode) 1011: 25Hz (LP or LN mode) 1100: 12.5Hz (LP or LN mode) 1101: 6.25Hz (LP mode) 1110: 3.125Hz (LP mode) 1111: 1.5625Hz (LP mode) Can be changed on-the-fly.

16.28 FIFO_CONFIG0

Name: FIFO_CONFIG0
Address: 29 (1Dh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	FIFO_MODE	Set the FIFO operation mode. 00: Bypass (disabled) 01: Stream mode - Frames are overwritten when the FIFO full condition is reached. Supported only for 8, 16, 20 bytes frame size. When this mode is selected for 32 or 64 bytes frame sizes, FIFO remains in Bypass mode. 10: Stop-on-full mode - Frames are not stored in FIFO once the FIFO full condition is reached. 11: Reserved Can be changed on-the-fly.
5:0	FIFO_DEPTH	Set the FIFO depth in bytes. 000111: Sets FIFO depth to 2K bytes (recommended setting) 011111: Sets FIFO depth to 8K bytes (valid when all APEX features are disabled) Others: Reserved Can be changed when FIFO is disabled (Bypass mode).

16.29 FIFO_CONFIG1_0

Name: FIFO_CONFIG1_0
Address: 30 (1Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FIFO_WM_TH[7:0]	Lower bits of FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. Can be changed on-the-fly.

16.30 FIFO_CONFIG1_1

Name: FIFO_CONFIG1_1
Address: 31 (1Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FIFO_WM_TH[15:8]	Upper bits of FIFO watermark threshold. When set to 0, the watermark is disabled. When writing new threshold value, user must first write threshold LSByte (bits [7:0]), then MSByte (bits [15:8]). New threshold register value will take effect only when MSByte is written. Can be changed on-the-fly.

16.31 FIFO_CONFIG2

Name: FIFO_CONFIG2
Address: 32 (20h)
Serial IF: R/W
Reset value: 0x20
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	FIFO_FLUSH	FIFO flush command. When set high the FIFO is flushed, meaning the pointers and control logic is reset. Configuration registers are not reset. Can be changed on-the-fly.
6:4	-	Reserved
3	FIFO_WR_WM_GT_TH	Set write watermark interrupt generating condition: 0: Write watermark interrupt generated when FIFO data count is equal to the FIFO watermark threshold 1: Write watermark interrupt generated when FIFO data count is greater than or equal to FIFO watermark threshold Can be changed when FIFO is disabled (Bypass mode).
2:0	-	Reserved

16.32 FIFO_CONFIG3

Name: FIFO_CONFIG3
Address: 33 (21h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	FIFO_ES1_EN	Enable External Sensor 1 data insertion into FIFO frame
4	FIFO_ES0_EN	Enable External Sensor 0 data insertion into FIFO frame
3	FIFO_HIRES_EN	Enable high resolution accel and gyro data insertion into FIFO frame
2	FIFO_GYRO_EN	Enable gyro data insertion into FIFO frame
1	FIFO_ACCEL_EN	Enable accel data insertion into FIFO frame
0	FIFO_IF_EN	Enable Sensor Registers write interface to FIFO. This interface should be enabled when the FIFO is also enabled (i.e., not in bypass mode). A standard enable sequence is: 1) Enable FIFO. 2) Enable Sensor Registers to FIFO interface. The opposite sequence should be used for the disable. To prevent power drain, FIFO_IF_EN should be set to 0 if FIFO is in bypass mode. Can be changed on-the-fly.

16.33 FIFO_CONFIG4

Name: FIFO_CONFIG4
Address: 34 (22h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	FIFO_COMP_NC_FLOW_CFG	Configures the compression algorithm to write non-compressed packets to FIFO at a certain rate 000: Non-compressed packet flow is disabled 001: Non-compressed packet every 8 frames 010: Non-compressed packet every 16 frames 011: Non-compressed packet every 32 frames 100: Non-compressed packet every 64 frames 101: Non-compressed packet every 128 frames Others: Reserved
2	FIFO_COMP_EN	0: FIFO compression disabled 1: FIFO compression enabled
1	FIFO_TMST_FSYNC_EN	Enable the insertion of the Timestamp or FSYNC data into FIFO frame 0: No Timestamp/FSYNC data inserted into FIFO frame (timestamp fields are 0x0000). FSYNC_TAG_EN bit in FIFO header is 0. 1: Timestamp/FSYNC data inserted into FIFO frame. FSYNC_TAG_EN bit in FIFO header is set on an FSYNC trigger event.
0	FIFO_ES0_6B_9B	Select number of valid bytes provided by External Sensor 0 0: 6 bytes 1: 9 bytes

16.34 TMST_WOM_CONFIG

Name: TMST_WOM_CONFIG
Address: 35 (23h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	TMST_DELTA_EN	Time Stamp Delta Enable 0: Time stamp field does not contain the measurement of time since the last occurrence of trigger event 1: Time stamp field contains the measurement of time since the last occurrence of trigger event
5	TMST_RESOL	Time Stamp Resolution 0: 1µs 1: 16µs
4	WOM_EN	Wake on Motion Enable 0: Wake on Motion not enabled 1: Wake on Motion enabled
3	WOM_MODE	Wake on Motion Mode 0: Initial sample is stored. Future samples are compared to initial sample 1: Compare current sample to previous sample
2	WOM_INT_MODE	Wake on Motion Interrupt 0: Off 1: On
1:0	WOM_INT_DUR	Wake on Motion Interrupt Duration 00: Wake on Motion interrupt asserted at first over-threshold event 01: Wake on Motion interrupt asserted at second over-threshold event 10: Wake on Motion interrupt asserted at third over-threshold event 11: Wake on Motion interrupt asserted at fourth over-threshold event

16.35 FSYNC_CONFIG0

Name: FSYNC_CONFIG0
Address: 36 (24h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3	AP_FSYNC_FLAG_CLEAR_SEL	Select the AP/UI FSYNC flag clear policy. 0: The FSYNC flag is cleared when UI/AP sensor register is updated. 1: The FSYNC flag is cleared when UI/AP serial interface reads the sensor register LSB of FSYNC tagged axis.
2:0	AP_FSYNC_SEL	Select the AP/UI sensor that will carry the FSYNC tagging. 0: FSYNC tagging is disabled 1: Tag FSYNC flag to TEMP_DATA_UI LSB 2: Tag FSYNC flag to GYRO_DATA_X_UI LSB 3: Tag FSYNC flag to GYRO_DATA_Y_UI LSB 4: Tag FSYNC flag to GYRO_DATA_Z_UI LSB 5: Tag FSYNC flag to ACCEL_DATA_X_UI LSB 6: Tag FSYNC flag to ACCEL_DATA_Y_UI LSB 7: Tag FSYNC flag to ACCEL_DATA_Z_UI LSB

16.36 DMP_EXT_SEN_ODR_CFG

Name: DMP_EXT_SEN_ODR_CFG
Address: 39 (27h)
Serial IF: R/W
Reset value: 0x01
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	EXT_SENSOR_EN	0: Disables generation of ODR event for external sensor operation per the setting of EXT_ODR. 1: Enables generation of ODR event for external sensor operation per the setting of EXT_ODR.
5:3	EXT_ODR	I^2C master external sensor ODR 000: 3.125Hz 001: 6.25Hz 010: 12.5Hz 011: 25Hz 100: 50Hz 101: 100Hz 110: 200Hz 111: 400Hz
2:0	APEX_ODR	DMP Output Data Rate. APEX_ODR should be smaller than or equal to both ACCEL_ODR and GYRO_ODR. All rates shown below except 800Hz can be set if Accel UI/AP in in LP mode. Accel UI/AP must be in LN mode to set 800Hz. 000: 25Hz 001: 50Hz 010: 100Hz 011: 200Hz 100: 400Hz 101: 800Hz 110: Reserved 111: Reserved

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16.37 ODR_DECIMATE_CONFIG

Name: ODR_DECIMATE_CONFIG
Address: 40 (28h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	GYRO_FIFO_ODR_DEC	Decimation factor for Gyroscope FIFO data: 0000: 1 (same are input ODR) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: Reserved 1110: Reserved 1111: Reserved
3:0	ACCEL_FIFO_ODR_DEC	Decimation factor for Accelerometer FIFO data: 0000: 1 (same are input ODR) 0001: 2 0010: 4 0011: 8 0100: 16 0101: 32 0110: 64 0111: 128 1000: 256 1001: 512 1010: 1024 1011: 2048 1100: 4096 1101: Reserved 1110: Reserved 1111: Reserved

16.38 EDMP_APEX_EN0

Name: EDMP_APEX_EN0
Address: 41 (29h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	RESERVED4	Reserved for future use - Set 1 to enable eDMP to run extended custom algorithm from RAM image
6	RESERVED3	Reserved for future use - Set 1 to enable eDMP to run extended custom algorithm from RAM image
5	FF_EN	Set 1 to enable Freefall algorithm
4	RESERVED2	Reserved for future use - Set 1 to enable eDMP to run extended custom algorithm from RAM image
3	RESERVED1	Reserved for future use - Set 1 to enable eDMP to run extended custom algorithm from RAM image
2	RESERVED0	Reserved for future use - Set 1 to enable eDMP to run extended custom algorithm from RAM image
1	SIF_EN	Set 1 to enable SIF algorithm
0	TAP_EN	Set 1 to enable Tap algorithm

16.39 EDMP_APEX_EN1

Name: EDMP_APEX_EN1
Address: 42 (2Ah)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	EDMP_ENABLE	Set 1 to enable eDMP
5	FEATURE3_EN	Set 1 to enable eDMP to run algorithms from RAM image
4	GAF_EN	Set 1 to enable GAF
3	-	Reserved
2	POWER_SAVE_EN	Set 1 to enable power save mode
1	INIT_EN	This bit is set by the host to indicate: eDMP executes only the segment of code that initialize constants used by algorithms.
0	SOFT_HARD_IRON_CORR_EN	Set 1 to enable soft iron hard iron correction

16.40 APEX_BUFFER_MGMT

Name: APEX_BUFFER_MGMT
Address: 43 (2Bh)
Serial IF: R/W (bits 5:4 are R only)
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	FF_DURATION_HOST_RPTR	LSB indicates SRAM address for host to read; MSB indicates size 2 buffer wrap around 00: Host reads buffer 0 01: Host reads buffer 1 10: Host reads buffer 0 11: Host reads buffer 1
5:4	FF_DURATION_EDMP_WPTR	Read only register field: LSB indicates SRAM address for eDMP to write; MSB indicates size 2 buffer wrap around 00: eDMP writes to buffer 0 01: eDMP writes to buffer 1 10: eDMP writes to buffer 0 11: eDMP writes to buffer 1
3:0	-	Reserved

16.41 INTF_CONFIG0

Name: INTF_CONFIG0
Address: 44 (2Ch)
Serial IF: R/W (bits 1 and 0 are Read only)
Reset value: 0x8A
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	AP_SPI_34_MODE	Read only register field, shows OTP trim for UI interface SPI in 3-wire or 4-wire mode 0: 3-wire mode 1: 4-wire mode
0	AP_SPI_MODE	Read only register field, shows OTP trim for UI interface SPI mode selection 0: SPI mode 0 or 3 1: SPI mode 1 or 2

16.42 INTF_CONFIG1_OVRD

Name: INTF_CONFIG1_OVRD
Address: 45 (2Dh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3	AP_SPI_34_MODE_OVRD	0: Override disable for AP interface SPI 4-wire/3-wire modes 1: Override enable for AP interface SPI 4-wire/3-wire modes
2	AP_SPI_34_MODE_OVRD_VAL	Override value for AP interface SPI 4-wire/3-wire modes 0: SPI 3-wire mode 1: SPI 4-wire mode
1	AP_SPI_MODE_OVRD	0: Override disable for AP interface SPI_MODE value 1: Override enable for AP interface SPI_MODE value
0	AP_SPI_MODE_OVRD_VAL	Override value for AP interface SPI Mode 0: SPI mode 0 or 3 1: SPI mode 1 or 2

16.43 IOC_PAD_SCENARIO

Name: IOC_PAD_SCENARIO
Address: 47 (2Fh)
Serial IF: R
Reset value: 0x03
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:1	AUX1_MODE	Read only register field, effective only when AUX1_ENABLE is 1. Selects AUX1 mode: 00: Reserved 01: AUX1 in I2C Master mode 10: AUX1 in I2C Master Bypass mode (Enable only when AP is not in SPI mode) 11: Reserved
0	AUX1_ENABLE	Read only register field, enable or disable AUX1 0: AUX1 disabled 1: AUX1 enabled

16.44 IOC_PAD_SCENARIO_AUX_OVRD

Name: IOC_PAD_SCENARIO_AUX_OVRD
Address: 48 (30h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:5	-	Reserved
4	AUX1_MODE_OVRD	Override enable for AUX1_MODE 0: Disable 1: Enable
3:2	AUX1_ENABLE_OVRD_VAL	Override value for AUX1_ENABLE. Effective only when AUX1_ENABLE is 1. Selects modes of AUX1 use: 0: Reserved 1: AUX1 in I2C Master mode 2: AUX1 in I2C Master Bypass mode (enable only when AP is not in SPI mode) Note: When enabling the I2C Master Bypass mode, this register should be programmed individually, not as part of a burst transaction.
1	AUX1_ENABLE_OVRD	Override enable for AUX1_ENABLE 0: Disable 1: Enable
0	AUX1_ENABLE_OVRD_VAL	Override value for AUX1_ENABLE 0: AUX1 disabled 1: AUX1 enabled

16.45 DRIVE_CONFIG0

Name: DRIVE_CONFIG0
Address: 50 (32h)
Serial IF: R/W
Reset value: 0x6A
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6:4	PADS_I2C_SLEW	Slew rate control for any pin in the I^2C mode of operation, including pins on the AP serial interface when device is a client device of an I^2C bus, including pins on the AUX1 serial interface when device is a master device of an I^2C bus. Setting of the slew rate takes effect 1.5µs after the register is programmed. 100: MIN: 3 ns; TYP: 20 ns; MAX: 136 ns 110: MIN: 2 ns; TYP: 7 ns; MAX: 84 ns Others: Reserved
3:1	PADS_SPI_SLEW	Slew rate control for any pin in the SPI mode of operation. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns
0	-	Reserved

16.46 DRIVE_CONFIG1

Name: DRIVE_CONFIG1
Address: 51 (33h)
Serial IF: R/W
Reset value: 0x2D
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	PADS_I3C_DDR_SLEW	Slew rate control when device is in I3C^{SM} DDR protocol. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns
2:0	PADS_I3C_SDR_SLEW	Slew rate control when device is in I3C^{SM} SDR protocol. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns

16.47 DRIVE_CONFIG2

Name: DRIVE_CONFIG2
Address: 52 (34h)
Serial IF: R/W
Reset value: 0x02
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	PADS_SLEW	Slew rate control for INT1 pin at all times. Slew rate control for all pins before OTP copy operation is completed. Setting of the slew rate takes effect 1.5µs after the register is programmed. 000: MIN: 12 ns; TYP: 38 ns; MAX: 106 ns 001: MIN: 4 ns; TYP: 14 ns; MAX: 45 ns 010: MIN: 3 ns; TYP: 10 ns; MAX: 37 ns 011: MIN: 2 ns; TYP: 7 ns; MAX: 25 ns 100: MIN: 1 ns; TYP: 5 ns; MAX: 17 ns 101: MIN: 1 ns; TYP: 4 ns; MAX: 14 ns 11x: MIN: 0.1 ns; TYP: 0.5 ns; MAX: 6 ns

16.48 REG_MISC1

Name: REG_MISC1
Address: 53 (35h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	OSC_ID_OVRD	Selects MCLK source. 0000: MCLK source requested by internal logic (default) 0010: Requests internal relaxation oscillator 1000: Requests external clock Rest: Reserved The selected clock source is the highest index that's requested and that is ready.

16.49 INT_APEX_CONFIG0

Name: INT_APEX_CONFIG0
Address: 57 (39h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT_STATUS_MASK_PIN_EXT2_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext2_det status bit from INT_APEX_STATUS0 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
6	INT_STATUS_MASK_PIN_FF_DET	Enable interrupt pin assertion when the INT_STATUS_FF_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
5	INT_STATUS_MASK_PIN_EXT1_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext1_det status bit from INT_APEX_STATUS0 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
4	INT_STATUS_MASK_PIN_EXT0_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext0_det status bit from INT_APEX_STATUS0 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
3	INT_STATUS_MASK_PIN_SIF_DET	For the SIF detection event, this is to enable the interrupt pin assertion when the int_status_sif_detect status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
2	INT_STATUS_MASK_PIN_LOW_G_DET	Enable interrupt pin assertion when the INT_STATUS_LOW_G_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
1	INT_STATUS_MASK_PIN_HIGH_G_DET	Enable interrupt pin assertion when the INT_STATUS_HIGH_G_DET status bit is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
0	INT_STATUS_MASK_PIN_TAP_DET	Enable interrupt pin assertion when the INT_STATUS_TAP_DET status bit is 1.

		0: Enable Interrupt pin assertion 1: No Interrupt pin assertion

16.50 INT_APEX_CONFIG1

Name: INT_APEX_CONFIG1
Address: 58 (3Ah)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT_STATUS_MASK_PIN_EXT6_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext6_det status bit from INT_APEX_STATUS1 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
5	INT_STATUS_MASK_PIN_EXT5_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext5_det status bit from INT_APEX_STATUS1 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
4	INT_STATUS_MASK_PIN_SA_DONE	0: Enable interrupt generation when Secure Authentication is done 1: Disable interrupt generation for Secure Authentication
3	-	Reserved
2	INT_STATUS_MASK_PIN_SELFTEST_DONE	0: Enable interrupt generation when self-test is done 1: Disable interrupt generation for self-test
1	INT_STATUS_MASK_PIN_EXT4_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext4_det status bit from INT_APEX_STATUS1 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion
0	INT_STATUS_MASK_PIN_EXT3_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling, this is to enable the interrupt pin assertion when the int_status_ext3_det status bit from INT_APEX_STATUS1 is 1. 0: Enable Interrupt pin assertion 1: No Interrupt pin assertion

16.51 INT_APEX_STATUS0

Name: INT_APEX_STATUS0
Address: 59 (3Bh)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT_STATUS_EXT2_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext2 Detection interrupt did not occur. 1: Ext2 Detection interrupt occurred.
6	INT_STATUS_FF_DET	0: Freefall interrupt did not occur. 1: Freefall interrupt occurred.
5	INT_STATUS_EXT1_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext1 Detection interrupt did not occur. 1: Ext1 Detection interrupt occurred.
4	INT_STATUS_EXT0_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext0 Detection interrupt did not occur. 1: Ext0 Detection interrupt occurred.
3	INT_STATUS_SIF_DET	0: SIF Detection interrupt did not occur. 1: SIF Detection interrupt occurred.
2	INT_STATUS_LOW_G_DET	0: LowG Detection interrupt did not occur. 1: LowG Detection interrupt occurred.
1	INT_STATUS_HIGH_G_DET	0: HighG Detection interrupt did not occur. 1: HighG Detection interrupt occurred.
0	INT_STATUS_TAP_DET	0: Tap Detection interrupt did not occur. 1: Tap Detection interrupt occurred.

16.52 INT_APEX_STATUS1

Name: INT_APEX_STATUS1
Address: 60 (3Ch)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT_STATUS_EXT6_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext6 Detection interrupt did not occur. 1: Ext6 Detection interrupt occurred.
5	INT_STATUS_EXT5_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext5 Detection interrupt did not occur. 1: Ext5 Detection interrupt occurred.
4	INT_STATUS_SA_DONE	For EDMP_OUT interface. 0: Secure Authentication interrupt did not occur. 1: Secure Authentication interrupt occurred.
3	-	Reserved
2	INT_STATUS_SELFTEST_DONE	0: Self-Test interrupt did not occur. 1: Self-Test interrupt occurred.
1	INT_STATUS_EXT4_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext4 Detection interrupt did not occur. 1: Ext4 Detection interrupt occurred.
0	INT_STATUS_EXT3_DET	Reserved for future use – If custom algorithm run from RAM image requires event detection signaling. 0: Ext3 Detection interrupt did not occur. 1: Ext3 Detection interrupt occurred.

16.53 INT2_CONFIG0

Name: INT2_CONFIG0
Address: 86 (56h)
Serial IF: R/W
Reset value: 0x80
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT2_STATUS_EN_RESET_DONE	Enable interrupt status bit to flag the occurrence of Reset Done event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
6	INT2_STATUS_EN_AUX1_AGC_RDY	Enable interrupt status bit to flag the occurrence of AUX1 AGC Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
5	INT2_STATUS_EN_AP_AGC_RDY	Enable interrupt status bit to flag the occurrence of UI AGC Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
4	INT2_STATUS_EN_AP_FSYNC	Enable interrupt status bit to flag the occurrence of UI FSYNC event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
3	INT2_STATUS_EN_AUX1_DRDY	Enable interrupt status bit to flag the occurrence of AUX1 Data Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
2	INT2_STATUS_EN_DRDY	Enable interrupt status bit to flag the occurrence of UI Data Ready event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
1	INT2_STATUS_EN_FIFO_THS	Enable interrupt status bit to flag the occurrence of FIFO count ≥ FIFO threshold event on INT2

		0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.
0	INT2_STATUS_EN_FIFO_FULL	Enable interrupt status bit to flag the occurrence of FIFO full event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI or AUX1 interface.

16.54 INT2_CONFIG1

Name: INT2_CONFIG1
Address: 87 (57h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT2_STATUS_EN_APEX_EVENT	Enable interrupt status bit to flag the occurrence of APEX event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
5	INT2_STATUS_EN_I2CM_DONE	Enable interrupt status bit to flag the completion of I^2C master event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
4	INT2_STATUS_EN_I3C_PROTOCOL_ERR	Enable interrupt status bit to flag the occurrence of I3C Protocol Error event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
3	INT2_STATUS_EN_WOM_Z	Enable interrupt status bit to flag the occurrence of WOM on Z-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
2	INT2_STATUS_EN_WOM_Y	Enable interrupt status bit to flag the occurrence of WOM on Y-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
1	INT2_STATUS_EN_WOM_X	Enable interrupt status bit to flag the occurrence of WOM on X-axis event on INT2 0: Disable interrupt. 1: Enable interrupt. Setting can be changed by UI interface.
0	INT2_STATUS_EN_PLL_RDY	Enable interrupt status bit to flag the occurrence of PLL Ready event on INT2 0: Disable interrupt.

		1: Enable interrupt. Setting can be changed by UI interface.

16.55 INT2_CONFIG2

Name: INT2_CONFIG2
Address: 88 (58h)
Serial IF: R/W
Reset value: 0x04
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2	INT2_DRIVE	Sets INT2 to open-drain or push-pull 0: Push-pull 1: Open-drain
1	INT2_MODE	INT2 interrupt mode 0: Pulse mode 1: Latch mode Setting can be changed only when all interrupts of the corresponding serial interface are disabled
0	INT2_POLARITY	INT2 interrupt polarity 0: Active low 1: Active high Setting can be changed only when all interrupts of the corresponding serial interface are disabled

16.56 INT2_STATUS0

Name: INT2_STATUS0
Address: 89 (59h)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	INT2_STATUS_RESET_DONE	Flags the occurrence of Reset Done event on INT2 0: Interrupt did not occur 1: Interrupt occurred
6	INT2_STATUS_AUX1_AGC_RDY	Flags the occurrence of AUX1 AGC Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred
5	INT2_STATUS_AP_AGC_RDY	Flags the occurrence of UI AGC Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred
4	INT2_STATUS_AP_FSYNC	Flags the occurrence of UI FSYNC event on INT2 0: Interrupt did not occur 1: Interrupt occurred
3	INT2_STATUS_AUX1_DRDY	Flags the occurrence of AUX1 Data Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred
2	INT2_STATUS_DRDY	Flags the occurrence of UI Data Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred
1	INT2_STATUS_FIFO_THS	Flags the occurrence of FIFO count ≥ FIFO threshold event on INT2 0: Interrupt did not occur 1: Interrupt occurred
0	INT2_STATUS_FIFO_FULL	Flags the occurrence of FIFO full event on INT2 0: Interrupt did not occur 1: Interrupt occurred

16.57 INT2_STATUS1

Name: INT2_STATUS1
Address: 90 (5Ah)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	INT2_STATUS_APEX_EVENT	Flags the occurrence of APEX event on INT2 0: Interrupt did not occur 1: Interrupt occurred
5	INT2_STATUS_I2CM_DONE	Flags the occurrence of I^2C Master Done event on INT2 0: Interrupt did not occur 1: Interrupt occurred
4	INT2_STATUS_I3C_PROTOCOL_ERR	Flags the occurrence of $I3C^{SM}$ Protocol Error event on INT2 0: Interrupt did not occur 1: Interrupt occurred
3	INT2_STATUS_WOM_Z	Flags the occurrence of Z-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred
2	INT2_STATUS_WOM_Y	Flags the occurrence of Y-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred
1	INT2_STATUS_WOM_X	Flags the occurrence of X-axis WOM event on INT2 0: Interrupt did not occur 1: Interrupt occurred
0	INT2_STATUS_PLL_RDY	Flags the occurrence of PLL Ready event on INT2 0: Interrupt did not occur 1: Interrupt occurred

16.58 WHO_AM_I

Name: WHO_AM_I
Address: 114 (72h)
Serial IF: R
Reset value: 0x81
Clock Domain: ALL

BIT	NAME	FUNCTION
7:0	WHOAMI	Register to indicate to user which device is being accessed

Description:

This register is used to verify the identity of the device. The contents of WHOAMI is an 8-bit device ID. The default value of the register is 0x81. This is different from the I^2C address of the device as seen on the slave I^2C controller by the applications processor.

16.59 REG_HOST_MSG

Name: REG_HOST_MSG
Address: 115 (73h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	EDMP_ON_DEMAND_EN	When set, a trigger will be sent which will cause the eDMP to run once. It is automatically reset to 0.
4:1	-	Reserved
0	TESTOPENABLE	1: Enable test operation

16.60 IREG_ADDR_15_8

Name: IREG_ADDR_15_8
Address: 124 (7Ch)
Serial IF: R/W
Reset value: Variable, depends on device usage history
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	IREG_ADDR_15_8	Address bit[15:8] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly.

16.61 IREG_ADDR_7_0

Name: IREG_ADDR_7_0
Address: 125 (7Dh)
Serial IF: R/W
Reset value: Variable, depends on device usage history
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	IREG_ADDR_7_0	Address bit[7:0] of the 16-bit indirect address for assessing indirect access registers (IREG) Can be changed on-the-fly.

16.62 IREG_DATA

Name: IREG_DATA
Address: 126 (7Eh)
Serial IF: R/W
Reset value: Variable, depends on device usage history
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:0	IREG_DATA	Register for indirect access registers (IREG) data read/write operations. Can be changed on-the-fly.

16.63 REG_MISC2

Name: REG_MISC2
Address: 127 (7Fh)
Serial IF: R/W
Reset value: 0x01
Clock Domain: SCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	SOFT_RST	0: Soft reset not enabled. 1: Triggers soft reset operation. The programmed value of 1 is self-cleared to 0 upon completion of soft reset operation. Can be changed on-the-fly.
0	IREG_DONE	0: Indicates that an indirect register access operation is in progress. No new indirect register access should be triggered. 1: Indirect register access has completed. New indirect register access can be triggered.

17 USER BANK IMEM_SRAM REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

17.1 IMEM_SRAM_REG_0

Name: IMEM_SRAM_REG_0
Address: 00 (00h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_X_STR_FT[7:0]	Self-test response for gyro X-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.2 IMEM_SRAM_REG_1

Name: IMEM_SRAM_REG_1
Address: 01 (01h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_X_STR_FT[15:8]	Self-test response for gyro X-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.3 IMEM_SRAM_REG_2

Name: IMEM_SRAM_REG_2
Address: 02 (02h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Y_STR_FT[7:0]	Self-test response for gyro Y-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.4 IMEM_SRAM_REG_3

Name: IMEM_SRAM_REG_3
Address: 03 (03h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Y_STR_FT[15:8]	Self-test response for gyro Y-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.5 IMEM_SRAM_REG_4

Name: IMEM_SRAM_REG_4
Address: 04 (04h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Z_STR_FT[7:0]	Self-test response for gyro Z-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.6 IMEM_SRAM_REG_5

Name: IMEM_SRAM_REG_5
Address: 05 (05h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Z_STR_FT[15:8]	Self-test response for gyro Z-axis. Units are in kdps. Full scale is 0.5kdps, LSB is 30mdps.

17.7 IMEM_SRAM_REG_6

Name: IMEM_SRAM_REG_6
Address: 06 (06h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_X_CMOS_GAIN_FT[7:0]	Gyro X-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.8 IMEM_SRAM_REG_7

Name: IMEM_SRAM_REG_7
Address: 07 (07h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	GYRO_X_CMOS_GAIN_FT[11:8]	Gyro X-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.9 IMEM_SRAM_REG_8

Name: IMEM_SRAM_REG_8
Address: 08 (08h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Y_CMOS_GAIN_FT[7:0]	Gyro Y-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.10 IMEM_SRAM_REG_9

Name: IMEM_SRAM_REG_9
Address: 09 (09h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	GYRO_Y_CMOS_GAIN_FT[11:8]	Gyro Y-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.11 IMEM_SRAM_REG_10

Name: IMEM_SRAM_REG_10
Address: 10 (0Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Z_CMOS_GAIN_FT[7:0]	Gyro Z-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.12 IMEM_SRAM_REG_11

Name: IMEM_SRAM_REG_11
Address: 11 (0Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	GYRO_Z_CMOS_GAIN_FT[11:8]	Gyro Z-axis gain measurement result. Units are in kdps. FSR is 500 dps, resolution is 122 mdps.

17.13 IMEM_SRAM_REG_12

Name: IMEM_SRAM_REG_12
Address: 12 (0Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_X_STR_FT[7:0]	Self-test response for accel X-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

17.14 IMEM_SRAM_REG_13

Name: IMEM_SRAM_REG_13
Address: 13 (0Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_X_STR_FT[15:8]	Self-test response for accel X-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

17.15 IMEM_SRAM_REG_14

Name: IMEM_SRAM_REG_14
Address: 14 (0Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Y_STR_FT[7:0]	Self-test response for accel Y-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

17.16 IMEM_SRAM_REG_15

Name: IMEM_SRAM_REG_15
Address: 15 (0Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Y_STR_FT[15:8]	Self-test response for accel Y-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

17.17 IMEM_SRAM_REG_16

Name: IMEM_SRAM_REG_16
Address: 16 (10h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Z_STR_FT[7:0]	Self-test response for accel Z-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

17.18 IMEM_SRAM_REG_17

Name: IMEM_SRAM_REG_17
Address: 17 (11h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Z_STR_FT[15:8]	Self-test response for accel Z-axis. Units are in g. Full scale is 1g, LSB is 0.122mg.

18 USER BANK IMEM_SRAM_APEX REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM_APEX. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

18.1 IMEM_SRAM_APEX_REG_4

Name: IMEM_SRAM_APEX_REG_4
Address: 04 (04h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_DYNAMIC_SERVICE_REQUEST[7:0]	ISR1 on-demand service request ID Set bit 1 to request set GAF parameters Set bit 2 to request set GAF bias Default: 0 (no ISR1 service requested)

18.2 IMEM_SRAM_APEX_REG_5

Name: IMEM_SRAM_APEX_REG_5
Address: 05 (05h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	USE_CASE_BITMASK[7:0]	ISR1 init request service ID depending on system usecase Set bit 1 for usecase which does not require GAF Set bit 3 for usecase which does not require Free-Fall Set bit 4 for usecase which does not require TAP Default: 0 (initialize all algo)

18.3 IMEM_SRAM_APEX_REG_7

Name: IMEM_SRAM_APEX_REG_7
Address: 07 (07h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_NUM[7:0]	Type of the last reported TAP event: 0: no tap, 1: single tap, 2: double tap, 3:triple tap

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18.4 IMEM_SRAM_APEX_REG_8

Name: IMEM_SRAM_APEX_REG_8
Address: 08 (08h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_AXIS[7:0]	Indicate the axis of the tap in the device frame 0: ax, 1: ay, 2: az

18.5 IMEM_SRAM_APEX_REG_9

Name: IMEM_SRAM_APEX_REG_9
Address: 09 (09h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_DIR[7:0]	Indicate the direction of the tap in the device frame 0: positive, 1: negative

18.6 IMEM_SRAM_APEX_REG_64

Name: IMEM_SRAM_APEX_REG_64
Address: 64 (40h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	POWER_SAVE_TIME[7:0]	Time of inactivity after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400

18.7 IMEM_SRAM_APEX_REG_65

Name: IMEM_SRAM_APEX_REG_65
Address: 65 (41h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	POWER_SAVE_TIME[15:8]	Time of inactivity after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400

18.8 IMEM_SRAM_APEX_REG_66

Name: IMEM_SRAM_APEX_REG_66
Address: 66 (42h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	POWER_SAVE_TIME[23:16]	Time of inactivity after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400

18.9 IMEM_SRAM_APEX_REG_67

Name: IMEM_SRAM_APEX_REG_67
Address: 67 (43h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	POWER_SAVE_TIME[31:24]	Time of inactivity after which eDMP goes in power save mode. Unit: time in sample number Range: [0 - 4294967295] Default value: 6400

18.10 IMEM_SRAM_APEX_REG_280

Name: IMEM_SRAM_APEX_REG_280
Address: 280 (118h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_STATIC_SERVICE_REQUEST[7:0]	ISR2 on-demand service request ID Set bit 0 to request memset service Default: 0 (no ISR2 service requested)

18.11 IMEM_SRAM_APEX_REG_281

Name: IMEM_SRAM_APEX_REG_281
Address: 281 (119h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_STATIC_SERVICE_REQUEST[15:8]	ISR2 on-demand service request ID Set bit 0 to request memset service Default: 0 (no ISR2 service requested)

18.12 IMEM_SRAM_APEX_REG_282

Name: IMEM_SRAM_APEX_REG_282
Address: 282 (11Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_STATIC_SERVICE_REQUEST[23:16]	ISR2 on-demand service request ID Set bit 0 to request memset service Default: 0 (no ISR2 service requested)

18.13 IMEM_SRAM_APEX_REG_283

Name: IMEM_SRAM_APEX_REG_283
Address: 283 (11Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_STATIC_SERVICE_REQUEST[31:24]	ISR2 on-demand service request ID Set bit 0 to request memset service Default: 0 (no ISR2 service requested)

18.14 IMEM_SRAM_APEX_REG_284

Name: IMEM_SRAM_APEX_REG_284
Address: 284 (11Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_MEMSET_ADDR[7:0]	Start address of RAM area to be written by EDMP when requested by memset static service.

18.15 IMEM_SRAM_APEX_REG_285

Name: IMEM_SRAM_APEX_REG_285
Address: 285 (11Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_MEMSET_ADDR[15:8]	Start address of RAM area to be written by EDMP when requested by memset static service.

18.16 IMEM_SRAM_APEX_REG_286

Name: IMEM_SRAM_APEX_REG_286
Address: 286 (11Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_MEMSET_VALUE[7:0]	Value to be written by EDMP to RAM area when requested by memset static service.

18.17 IMEM_SRAM_APEX_REG_288

Name: IMEM_SRAM_APEX_REG_288
Address: 288 (120h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_MEMSET_SIZE[7:0]	Length in bytes of RAM area to be written by EDMP when requested by memset static service.

18.18 IMEM_SRAM_APEX_REG_289

Name: IMEM_SRAM_APEX_REG_289
Address: 289 (121h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ONDEMAND_MEMSET_SIZE[15:8]	Length in bytes of RAM area to be written by EDMP when requested by memset static service.

18.19 IMEM_SRAM_APEX_REG_312

Name: IMEM_SRAM_APEX_REG_312
Address: 312 (138h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_PDR_PARTITION[7:0]	SIF partition reconfiguration in case SIF PDR is not 50 Hz.

18.20 IMEM_SRAM_APEX_REG_313

Name: IMEM_SRAM_APEX_REG_313
Address: 313 (139h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_PDR_PARTITION[15:8]	SIF partition reconfiguration in case SIF PDR is not 50 Hz.

18.21 IMEM_SRAM_APEX_REG_314

Name: IMEM_SRAM_APEX_REG_314
Address: 314 (13Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_PDR_PARTITION[23:16]	SIF partition reconfiguration in case SIF PDR is not 50 Hz.

18.22 IMEM_SRAM_APEX_REG_315

Name: IMEM_SRAM_APEX_REG_315
Address: 315 (13Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_PDR_PARTITION[31:24]	SIF partition reconfiguration in case SIF PDR is not 50 Hz.

18.23 IMEM_SRAM_APEX_REG_340

Name: IMEM_SRAM_APEX_REG_340
Address: 340 (154h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_PDR_PARTITION[7:0]	GAF partition reconfiguration in case GAF PDR is not 50 Hz and mag ODR is not 50 Hz.

18.24 IMEM_SRAM_APEX_REG_341

Name: IMEM_SRAM_APEX_REG_341
Address: 341 (155h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_PDR_PARTITION[15:8]	GAF partition reconfiguration in case GAF PDR is not 50 Hz and mag ODR is not 50 Hz.

18.25 IMEM_SRAM_APEX_REG_342

Name: IMEM_SRAM_APEX_REG_342
Address: 342 (156h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_PDR_PARTITION[23:16]	GAF partition reconfiguration in case GAF PDR is not 50 Hz and mag ODR is not 50 Hz.

18.26 IMEM_SRAM_APEX_REG_343

Name: IMEM_SRAM_APEX_REG_343
Address: 343 (157h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_PDR_PARTITION[31:24]	GAF partition reconfiguration in case GAF PDR is not 50 Hz and mag ODR is not 50 Hz.

18.27 IMEM_SRAM_APEX_REG_392

Name: IMEM_SRAM_APEX_REG_392
Address: 392 (188h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	DMP_ODR_LAST_INIT[7:0]	Encoded eDMP ODR value effective during last eDMP init request 0x1 for eDMP ODR 25Hz 0x2 for eDMP ODR 50Hz 0x8 for eDMP ODR 100Hz 0x80 for eDMP ODR 200Hz 0x8000 for eDMP ODR 400Hz 0x80000000 for eDMP ODR 800Hz Other values are reserved

18.28 IMEM_SRAM_APEX_REG_393

Name: IMEM_SRAM_APEX_REG_393
Address: 393 (189h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	DMP_ODR_LAST_INIT[15:8]	Encoded eDMP ODR value effective during last eDMP init request 0x1 for eDMP ODR 25Hz 0x2 for eDMP ODR 50Hz 0x8 for eDMP ODR 100Hz 0x80 for eDMP ODR 200Hz 0x8000 for eDMP ODR 400Hz 0x80000000 for eDMP ODR 800Hz Other values are reserved

18.29 IMEM_SRAM_APEX_REG_394

Name: IMEM_SRAM_APEX_REG_394
Address: 394 (18Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	DMP_ODR_LAST_INIT[23:16]	Encoded eDMP ODR value effective during last eDMP init request 0x1 for eDMP ODR 25Hz 0x2 for eDMP ODR 50Hz 0x8 for eDMP ODR 100Hz 0x80 for eDMP ODR 200Hz 0x8000 for eDMP ODR 400Hz 0x80000000 for eDMP ODR 800Hz Other values are reserved

18.30 IMEM_SRAM_APEX_REG_395

Name: IMEM_SRAM_APEX_REG_395
Address: 395 (18Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	DMP_ODR_LAST_INIT[31:24]	Encoded eDMP ODR value effective during last eDMP init request 0x1 for eDMP ODR 25Hz 0x2 for eDMP ODR 50Hz 0x8 for eDMP ODR 100Hz 0x80 for eDMP ODR 200Hz 0x8000 for eDMP ODR 400Hz 0x80000000 for eDMP ODR 800Hz Other values are reserved

18.31 IMEM_SRAM_APEX_REG_428

Name: IMEM_SRAM_APEX_REG_428
Address: 428 (1ACh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[7:0]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.32 IMEM_SRAM_APEX_REG_429

Name: IMEM_SRAM_APEX_REG_429
Address: 429 (1ADh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[15:8]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.33 IMEM_SRAM_APEX_REG_430

Name: IMEM_SRAM_APEX_REG_430
Address: 430 (1AEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[23:16]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.34 IMEM_SRAM_APEX_REG_431

Name: IMEM_SRAM_APEX_REG_431
Address: 431 (1AFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[31:24]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.35 IMEM_SRAM_APEX_REG_432

Name: IMEM_SRAM_APEX_REG_432
Address: 432 (1B0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[39:32]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.36 IMEM_SRAM_APEX_REG_433

Name: IMEM_SRAM_APEX_REG_433
Address: 433 (1B1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[47:40]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.37 IMEM_SRAM_APEX_REG_434

Name: IMEM_SRAM_APEX_REG_434
Address: 434 (1B2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[55:48]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.38 IMEM_SRAM_APEX_REG_435

Name: IMEM_SRAM_APEX_REG_435
Address: 435 (1B3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[63:56]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.39 IMEM_SRAM_APEX_REG_436

Name: IMEM_SRAM_APEX_REG_436
Address: 436 (1B4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[71:64]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.40 IMEM_SRAM_APEX_REG_437

Name: IMEM_SRAM_APEX_REG_437
Address: 437 (1B5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[79:72]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.41 IMEM_SRAM_APEX_REG_438

Name: IMEM_SRAM_APEX_REG_438
Address: 438 (1B6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[87:80]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.42 IMEM_SRAM_APEX_REG_439

Name: IMEM_SRAM_APEX_REG_439
Address: 439 (1B7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[95:88]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.43 IMEM_SRAM_APEX_REG_440

Name: IMEM_SRAM_APEX_REG_440
Address: 440 (1B8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[103:96]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.44 IMEM_SRAM_APEX_REG_441

Name: IMEM_SRAM_APEX_REG_441
Address: 441 (1B9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[111:104]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.45 IMEM_SRAM_APEX_REG_442

Name: IMEM_SRAM_APEX_REG_442
Address: 442 (1BAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[119:112]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.46 IMEM_SRAM_APEX_REG_443

Name: IMEM_SRAM_APEX_REG_443
Address: 443 (1BBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[127:120]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.47 IMEM_SRAM_APEX_REG_444

Name: IMEM_SRAM_APEX_REG_444
Address: 444 (1BCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[135:128]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.48 IMEM_SRAM_APEX_REG_445

Name: IMEM_SRAM_APEX_REG_445
Address: 445 (1BDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GLOBAL_MOUNTING_MATRIX[143:136]	A q14 3x3 matrix applied to input accel and gyro data Default: Identity matrix being 0x4000 0 0 0 0x4000 0 0 0 0x4000

18.49 IMEM_SRAM_APEX_REG_446

Name: IMEM_SRAM_APEX_REG_446
Address: 446 (1BEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_MODE[7:0]	GAF configuration of eDMP system architecture. bit 0: - 0 if there is no mag (AG only) - 1 if there is ICT-1531x (calib mag will be run) bit 1: - 0 if there is no calib gyro expected (AM only) - 1 if there is calib gyro expected (calib gyro will be run) bit 2: - 0 if MRM sequence is disabled - 1 if automatic MRM is run depending on mag data value bit 3: - 0 if push in FIFO is to be made at GAF PDR (default) - 1 if no push in FIFO is to be done by DMP Default: 0x03 (calibration mag, calibration gyro, no auto MRM, push in FIFO

18.50 IMEM_SRAM_APEX_REG_449

Name: IMEM_SRAM_APEX_REG_449
Address: 449 (1C1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_ONDEMAND_MRM_REQUEST[7:0]	Request MRM to be run during next eDMP execution. Set to not null value to request MRM. Default: 0x0

18.51 IMEM_SRAM_APEX_REG_514

Name: IMEM_SRAM_APEX_REG_514
Address: 514 (202h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DURATION[7:0]	Duration of the freefall. Unit: number of samples. Freefall duration in seconds / ACCEL_ODR in Hz

18.52 IMEM_SRAM_APEX_REG_515

Name: IMEM_SRAM_APEX_REG_515
Address: 515 (203h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DURATION[15:8]	Duration of the freefall. Unit: number of samples. Freefall duration in seconds / ACCEL_ODR in Hz

18.53 IMEM_SRAM_APEX_REG_520

Name: IMEM_SRAM_APEX_REG_520
Address: 520 (208h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[7:0]	Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms)

18.54 IMEM_SRAM_APEX_REG_521

Name: IMEM_SRAM_APEX_REG_521
Address: 521 (209h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[15:8]	Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms)

18.55 IMEM_SRAM_APEX_REG_522

Name: IMEM_SRAM_APEX_REG_178
Address: 522 (20Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[23:16]	Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms)

18.56 IMEM_SRAM_APEX_REG_523

Name: IMEM_SRAM_APEX_REG_523
Address: 523 (20Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MIN_DURATION[31:24]	Minimum freefall duration. Shorter freefalls are ignored. Unit: time in samples number Range: [4 - 420] Default: 57 (set for default ODR = 400 Hz, equivalent to 142 ms)

18.57 IMEM_SRAM_APEX_REG_524

Name: IMEM_SRAM_APEX_REG_524
Address: 524 (20Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[7:0]	Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms)

18.58 IMEM_SRAM_APEX_REG_525

Name: IMEM_SRAM_APEX_REG_525
Address: 525 (20Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[15:8]	Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms)

18.59 IMEM_SRAM_APEX_REG_526

Name: IMEM_SRAM_APEX_REG_526
Address: 526 (20Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[23:16]	Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms)

18.60 IMEM_SRAM_APEX_REG_527

Name: IMEM_SRAM_APEX_REG_527
Address: 527 (20Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_MAX_DURATION[31:24]	Maximum freefall duration. Longer freefalls are ignored. Unit: time in samples number Range: [12 - 1040] Default: 285 (set for default ODR = 400 Hz, equivalent to 712 ms)

18.61 IMEM_SRAM_APEX_REG_528

Name: IMEM_SRAM_APEX_REG_528
Address: 528 (210h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION[7:0]	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s)

18.62 IMEM_SRAM_APEX_REG_529

Name: IMEM_SRAM_APEX_REG_529
Address: 529 (211h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION[15:8]	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s)

18.63 IMEM_SRAM_APEX_REG_530

Name: IMEM_SRAM_APEX_REG_530
Address: 530 (212h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [23:16]	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s)

18.64 IMEM_SRAM_APEX_REG_531

Name: IMEM_SRAM_APEX_REG_531
Address: 531 (213h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	FF_DEBOUNCE_DURATION [31:24]	Period after a freefall is signaled during which a new freefall will not be detected. Prevents false detection due to bounces. Unit: time in samples number Range: [75 - 3000] Default: 800 (set for default ODR = 800 Hz, equivalent to 1 s)

18.65 IMEM_SRAM_APEX_REG_536

Name: IMEM_SRAM_APEX_REG_536
Address: 536 (218h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH[7:0]	Threshold for accel values above which high-g state is detected. Unit: g in q12 Range: [1024 - 32768] Default: 29696

18.66 IMEM_SRAM_APEX_REG_537

Name: IMEM_SRAM_APEX_REG_537
Address: 537 (219h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH[15:8]	Threshold for accel values above which high-g state is detected. Unit: g in q12 Range: [1024 - 32768] Default: 29696

18.67 IMEM_SRAM_APEX_REG_538

Name: IMEM_SRAM_APEX_REG_538
Address: 538 (21Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH_HYST[7:0]	Hysteresis value subtracted from the high-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 640

18.68 IMEM_SRAM_APEX_REG_539

Name: IMEM_SRAM_APEX_REG_539
Address: 539 (21Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_PEAK_TH_HYST[15:8]	Hysteresis value subtracted from the high-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 640

18.69 IMEM_SRAM_APEX_REG_540

Name: IMEM_SRAM_APEX_REG_540
Address: 540 (21Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_TIME_TH[7:0]	The number of samples device should stay above (HIGHG_PEAK_TH + HIGHG_PEAK_TH_HYST) before HighG state is triggered. Unit: time in samples number Range: [1-300] Default: 1 (set for default ODR = 800 Hz, equivalent to 1.25 ms)

18.70 IMEM_SRAM_APEX_REG_541

Name: IMEM_SRAM_APEX_REG_541
Address: 541 (21Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	HIGHG_TIME_TH[15:8]	The number of samples device should stay above (HIGHG_PEAK_TH + HIGHG_PEAK_TH_HYST) before HighG state is triggered. Unit: time in samples number Range: [1-300] Default: 1 (set for default ODR = 800 Hz, equivalent to 1.25 ms)

18.71 IMEM_SRAM_APEX_REG_548

Name: IMEM_SRAM_APEX_REG_548
Address: 548 (224h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH[7:0]	Threshold for accel values below which low-g state is detected. Unit: g in q12 Range: [128 - 4096] Default: 2048

18.72 IMEM_SRAM_APEX_REG_549

Name: IMEM_SRAM_APEX_REG_549
Address: 549 (225h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH[15:8]	Threshold for accel values below which low-g state is detected. Unit: g in q12 Range: [128 - 4096] Default: 2048

18.73 IMEM_SRAM_APEX_REG_550

Name: IMEM_SRAM_APEX_REG_550
Address: 550 (226h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH_HYST[7:0]	Hysteresis value added to the low-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 128

18.74 IMEM_SRAM_APEX_REG_551

Name: IMEM_SRAM_APEX_REG_551
Address: 551 (227h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_PEAK_TH_HYST[15:8]	Hysteresis value added to the low-g threshold after exceeding it. Unit: g in q12 Range: [128 - 1024] Default: 128

18.75 IMEM_SRAM_APEX_REG_552

Name: IMEM_SRAM_APEX_REG_552
Address: 552 (228h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_TIME_TH[7:0]	Number of samples required to enter low-g state. Unit: time in samples number Range: [1 - 300] Default: 13 (set for default ODR = 800 Hz, equivalent to 16 ms)

18.76 IMEM_SRAM_APEX_REG_553

Name: IMEM_SRAM_APEX_REG_553
Address: 553 (229h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	LOWG_TIME_TH[15:8]	Number of samples required to enter low-g state. Unit: time in samples number Range: [1 - 300] Default: 13 (set for default ODR = 800 Hz, equivalent to 16 ms)

18.77 IMEM_SRAM_APEX_REG_560

Name: IMEM_SRAM_APEX_REG_560
Address: 560 (230h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_MIN_JERK[7:0]	The minimal value of jerk to be considered as a tap candidate. Unit: LSB with 1 LSB = 1g / 2^12 (of the jerk value) Range: [0 - 16384] Default: 4608 (equivalent to 1.125 g)

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18.78 IMEM_SRAM_APEX_REG_561

Name: IMEM_SRAM_APEX_REG_561
Address: 561 (231h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_MIN_JERK[15:8]	The minimal value of jerk to be considered as a tap candidate. Unit: LSB with 1 LSB = 1g / 2^12 (of the jerk value) Range: [0 - 16384] Default: 4608 (equivalent to 1.125 g)

18.79 IMEM_SRAM_APEX_REG_562

Name: IMEM_SRAM_APEX_REG_562
Address: 562 (232h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_TMAX[7:0]	Size of the analysis window to detect tap events (single, double or triple tap) Unit: time in sample number Range: [49 - 496] Default: 198 (set for default ODR = 400 Hz, equivalent to 0.495 s)

18.80 IMEM_SRAM_APEX_REG_563

Name: IMEM_SRAM_APEX_REG_563
Address: 563 (233h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_TMAX[15:8]	Size of the analysis window to detect tap events (single, double or triple tap) Unit: time in sample number Range: [49 - 496] Default: 198 (set for default ODR = 400 Hz, equivalent to 0.495 s)

18.81 IMEM_SRAM_APEX_REG_564

Name: IMEM_SRAM_APEX_REG_564
Address: 564 (234h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_TMIN[7:0]	Single tap window, sub-windows within Tmax to detect single-tap event. Unit: time in sample number Range: [24 - 184] Default: 66 (set for default ODR = 400 Hz, equivalent to 0.165 s)

18.82 IMEM_SRAM_APEX_REG_565

Name: IMEM_SRAM_APEX_REG_565
Address: 565 (235h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_SMUDGE_REJECT_THR[7:0]	Max acceptable number of samples (jerk value) over TAP_MAX_PEAK_TOL during the Tmin window. Over this value, Tap event is rejected Unit: time in number of samples Range: [13 - 92] Default: 34 (set for default ODR = 400 Hz, equivalent to 0.085 s)

18.83 IMEM_SRAM_APEX_REG_566

Name: IMEM_SRAM_APEX_REG_566
Address: 566 (236h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_MAX_PEAK_TOL[7:0]	Maximum peak tolerance is the percentage of pulse amplitude to get the smudge threshold for rejection Range: [1 (12.5%) 2 (25.0%) 3 (37.5%) 4 (50.0 %)] Default: 2

18.84 IMEM_SRAM_APEX_REG_567

Name: IMEM_SRAM_APEX_REG_567
Address: 567 (237h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_TAVG[7:0]	Energy measurement window size to determine the tap axis associated with the 1st tap. Unit: time in sample number Range: [1 ; 2 ; 4 ; 8] Default: 8

18.85 IMEM_SRAM_APEX_REG_568

Name: IMEM_SRAM_APEX_REG_568
Address: 568 (238h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_ODR[7:0]	Tap execution ODR: 0: 200Hz 1: 400Hz 2: 800Hz Default: 1 (400Hz)

18.86 IMEM_SRAM_APEX_REG_569

Name: IMEM_SRAM_APEX_REG_569
Address: 569 (239h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_MAX[7:0]	Maximal number of tap quantity detected to be valid. Range: [1 (single) ; 2 (double) ; 3 (triple)] Default: 2 (double tap)

18.87 IMEM_SRAM_APEX_REG_570

Name: IMEM_SRAM_APEX_REG_570
Address: 570 (23Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	TAP_MIN[7:0]	Minimal number of tap quantity detected to be valid. Range: [1 (single); 2 (double); 3 (triple)] Default: 2 (double tap)

18.88 IMEM_SRAM_APEX_REG_612

Name: IMEM_SRAM_APEX_REG_612
Address: 612 (264h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[7:0]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

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18.89 IMEM_SRAM_APEX_REG_613

Name: IMEM_SRAM_APEX_REG_613
Address: 613 (265h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[15:8]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.90 IMEM_SRAM_APEX_REG_614

Name: IMEM_SRAM_APEX_REG_614
Address: 614 (266h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[23:16]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.91 IMEM_SRAM_APEX_REG_615

Name: IMEM_SRAM_APEX_REG_615
Address: 615 (267h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[31:24]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.92 IMEM_SRAM_APEX_REG_616

Name: IMEM_SRAM_APEX_REG_616
Address: 616 (268h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[39:32]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.93 IMEM_SRAM_APEX_REG_617

Name: IMEM_SRAM_APEX_REG_617
Address: 617 (269h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[47:40]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.94 IMEM_SRAM_APEX_REG_618

Name: IMEM_SRAM_APEX_REG_618
Address: 618 (26Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[55:48]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.95 IMEM_SRAM_APEX_REG_619

Name: IMEM_SRAM_APEX_REG_619
Address: 619 (26Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[63:56]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.96 IMEM_SRAM_APEX_REG_620

Name: IMEM_SRAM_APEX_REG_620
Address: 620 (26Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[71:64]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.97 IMEM_SRAM_APEX_REG_621

Name: IMEM_SRAM_APEX_REG_621
Address: 621 (26Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[79:72]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.98 IMEM_SRAM_APEX_REG_622

Name: IMEM_SRAM_APEX_REG_622
Address: 622 (26Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[87:80]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.99 IMEM_SRAM_APEX_REG_623

Name: IMEM_SRAM_APEX_REG_623
Address: 623 (26Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[95:88]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.100 IMEM_SRAM_APEX_REG_624

Name: IMEM_SRAM_APEX_REG_624
Address: 624 (270h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[103:96]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.101 IMEM_SRAM_APEX_REG_625

Name: IMEM_SRAM_APEX_REG_625
Address: 625 (271h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[111:104]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.102 IMEM_SRAM_APEX_REG_626

Name: IMEM_SRAM_APEX_REG_626
Address: 626 (272h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[119:112]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.103 IMEM_SRAM_APEX_REG_627

Name: IMEM_SRAM_APEX_REG_627
Address: 627 (273h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[127:120]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.104 IMEM_SRAM_APEX_REG_628

Name: IMEM_SRAM_APEX_REG_628
Address: 628 (274h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[135:128]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.105 IMEM_SRAM_APEX_REG_629

Name: IMEM_SRAM_APEX_REG_629
Address: 629 (275h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[143:136]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.106 IMEM_SRAM_APEX_REG_630

Name: IMEM_SRAM_APEX_REG_630
Address: 630 (276h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[151:144]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.107 IMEM_SRAM_APEX_REG_631

Name: IMEM_SRAM_APEX_REG_631
Address: 631 (277h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[159:152]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.108 IMEM_SRAM_APEX_REG_632

Name: IMEM_SRAM_APEX_REG_632
Address: 632 (278h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[167:160]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.109 IMEM_SRAM_APEX_REG_633

Name: IMEM_SRAM_APEX_REG_633
Address: 633 (279h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[175:168]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.110 IMEM_SRAM_APEX_REG_634

Name: IMEM_SRAM_APEX_REG_634
Address: 634 (27Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[183:176]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.111 IMEM_SRAM_APEX_REG_635

Name: IMEM_SRAM_APEX_REG_635
Address: 635 (27Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[191:184]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.112 IMEM_SRAM_APEX_REG_636

Name: IMEM_SRAM_APEX_REG_636
Address: 636 (27Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[199:192]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.113 IMEM_SRAM_APEX_REG_637

Name: IMEM_SRAM_APEX_REG_637
Address: 637 (27Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[207:200]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.114 IMEM_SRAM_APEX_REG_638

Name: IMEM_SRAM_APEX_REG_638
Address: 638 (27Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[215:208]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.115 IMEM_SRAM_APEX_REG_639

Name: IMEM_SRAM_APEX_REG_639
Address: 639 (27Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[223:216]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.116 IMEM_SRAM_APEX_REG_640

Name: IMEM_SRAM_APEX_REG_640
Address: 640 (280h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[231:224]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.117 IMEM_SRAM_APEX_REG_641

Name: IMEM_SRAM_APEX_REG_641
Address: 641 (281h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[239:232]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.118 IMEM_SRAM_APEX_REG_642

Name: IMEM_SRAM_APEX_REG_642
Address: 642 (282h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[247:240]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.119 IMEM_SRAM_APEX_REG_643

Name: IMEM_SRAM_APEX_REG_643
Address: 643 (283h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[255:248]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.120 IMEM_SRAM_APEX_REG_644

Name: IMEM_SRAM_APEX_REG_644
Address: 644 (284h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[263:256]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.121 IMEM_SRAM_APEX_REG_645

Name: IMEM_SRAM_APEX_REG_645
Address: 645 (285h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[271:264]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.122 IMEM_SRAM_APEX_REG_646

Name: IMEM_SRAM_APEX_REG_646
Address: 646 (286h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[279:272]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.123 IMEM_SRAM_APEX_REG_647

Name: IMEM_SRAM_APEX_REG_647
Address: 647 (287h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_SOFTIRON_MATRIX[287:280]	A q30 3x3 matrix applied to input mag data Default: Identity matrix being 0x40000000 0 0 0 0x40000000 0 0 0 0x40000000

18.124 IMEM_SRAM_APEX_REG_648

Name: IMEM_SRAM_APEX_REG_648
Address: 648 (288h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_ODR_US[7:0]	GAF accelerometer input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.125 IMEM_SRAM_APEX_REG_649

Name: IMEM_SRAM_APEX_REG_649
Address: 649 (289h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_ODR_US[15:8]	GAF accelerometer input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.126 IMEM_SRAM_APEX_REG_650

Name: IMEM_SRAM_APEX_REG_650
Address: 650 (28Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_ODR_US[23:16]	GAF accelerometer input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.127 IMEM_SRAM_APEX_REG_651

Name: IMEM_SRAM_APEX_REG_651
Address: 651 (28Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_ODR_US[31:24]	GAF accelerometer input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.128 IMEM_SRAM_APEX_REG_652

Name: IMEM_SRAM_APEX_REG_652
Address: 652 (28Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_ODR_US[7:0]	GAF gyroscope input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.129 IMEM_SRAM_APEX_REG_653

Name: IMEM_SRAM_APEX_REG_653
Address: 653 (28Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_ODR_US[15:8]	GAF gyroscope input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.130 IMEM_SRAM_APEX_REG_654

Name: IMEM_SRAM_APEX_REG_654
Address: 654 (28Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_ODR_US[23:16]	GAF gyroscope input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.131 IMEM_SRAM_APEX_REG_655

Name: IMEM_SRAM_APEX_REG_655
Address: 655 (28Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_ODR_US[31:24]	GAF gyroscope input sensor data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.132 IMEM_SRAM_APEX_REG_656

Name: IMEM_SRAM_APEX_REG_656
Address: 656 (290h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_PDR_US[7:0]	GAF accelerometer processing data rate, sensor data are averaged if sensor is faster than GAF accelerometer PDR. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.133 IMEM_SRAM_APEX_REG_657

Name: IMEM_SRAM_APEX_REG_657
Address: 657 (291h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_PDR_US[15:8]	GAF accelerometer processing data rate, sensor data are averaged if sensor is faster than GAF accelerometer PDR. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.134 IMEM_SRAM_APEX_REG_658

Name: IMEM_SRAM_APEX_REG_658
Address: 658 (292h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_PDR_US[23:16]	GAF accelerometer processing data rate, sensor data are averaged if sensor is faster than GAF accelerometer PDR. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.135 IMEM_SRAM_APEX_REG_659

Name: IMEM_SRAM_APEX_REG_659
Address: 659 (293h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_PDR_US[31:24]	GAF accelerometer processing data rate, sensor data are averaged if sensor is faster than GAF accelerometer PDR. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.136 IMEM_SRAM_APEX_REG_660

Name: IMEM_SRAM_APEX_REG_660
Address: 660 (294h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_PDR_US[7:0]	GAF gyroscope processing data rate, sensor data are averaged if sensor is faster than GAF gyroscope PDR. Corresponds to GAF output data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.137 IMEM_SRAM_APEX_REG_661

Name: IMEM_SRAM_APEX_REG_661
Address: 661 (295h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_PDR_US[15:8]	GAF gyroscope processing data rate, sensor data are averaged if sensor is faster than GAF gyroscope PDR. Corresponds to GAF output data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.138 IMEM_SRAM_APEX_REG_662

Name: IMEM_SRAM_APEX_REG_662
Address: 662 (296h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_PDR_US[23:16]	GAF gyroscope processing data rate, sensor data are averaged if sensor is faster than GAF gyroscope PDR. Corresponds to GAF output data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.139 IMEM_SRAM_APEX_REG_663

Name: IMEM_SRAM_APEX_REG_663
Address: 663 (297h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_PDR_US[31:24]	GAF gyroscope processing data rate, sensor data are averaged if sensor is faster than GAF gyroscope PDR. Corresponds to GAF output data rate. Range: {1250;2500;5000;10000;20000} Unit: µs Default: 10000

18.140 IMEM_SRAM_APEX_REG_664

Name: IMEM_SRAM_APEX_REG_664
Address: 664 (298h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[7:0]	Duration of stationary detection. Unit: µs Default: 500000 (0.5 seconds)

18.141 IMEM_SRAM_APEX_REG_665

Name: IMEM_SRAM_APEX_REG_665
Address: 665 (299h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[15:8]	Duration of stationary detection. Unit: µs Default: 500000 (0.5 seconds)

18.142 IMEM_SRAM_APEX_REG_666

Name: IMEM_SRAM_APEX_REG_666
Address: 666 (29Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[23:16]	Duration of stationary detection. Unit: µs Default: 500000 (0.5 seconds)

18.143 IMEM_SRAM_APEX_REG_667

Name: IMEM_SRAM_APEX_REG_667
Address: 667 (29Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_DURATION_US[31:24]	Duration of stationary detection. Unit: µs Default: 500000 (0.5 seconds)

18.144 IMEM_SRAM_APEX_REG_668

Name: IMEM_SRAM_APEX_REG_668
Address: 668 (29Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[7:0]	Threshold on angular deviation for stationary detection. Unit: degree s32q16 Default: 65536 (1 degree)

18.145 IMEM_SRAM_APEX_REG_669

Name: IMEM_SRAM_APEX_REG_669
Address: 669 (29Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[15:8]	Threshold on angular deviation for stationary detection. Unit: degree s32q16 Default: 65536 (1 degree)

18.146 IMEM_SRAM_APEX_REG_670

Name: IMEM_SRAM_APEX_REG_670
Address: 670 (29Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[23:16]	Threshold on angular deviation for stationary detection. Unit: degree s32q16 Default: 65536 (1 degree)

18.147 IMEM_SRAM_APEX_REG_671

Name: IMEM_SRAM_APEX_REG_671
Address: 671 (29Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_THRESHOLD_DEG_Q16[31:24]	Threshold on angular deviation for stationary detection. Unit: degree s32q16 Default: 65536 (1 degree)

18.148 IMEM_SRAM_APEX_REG_672

Name: IMEM_SRAM_APEX_REG_672
Address: 672 (2A0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[7:0]	Gyroscope integration error related to bias precision. Higher value increases accel roll/pitch correction in steady state. Unit: LSB Default: 20

18.149 IMEM_SRAM_APEX_REG_673

Name: IMEM_SRAM_APEX_REG_673
Address: 673 (2A1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[15:8]	Gyroscope integration error related to bias precision. Higher value increases accel roll/pitch correction in steady state. Unit: LSB Default: 20

18.150 IMEM_SRAM_APEX_REG_674

Name: IMEM_SRAM_APEX_REG_674
Address: 674 (2A2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[23:16]	Gyroscope integration error related to bias precision. Higher value increases accel roll/pitch correction in steady state. Unit: LSB Default: 20

18.151 IMEM_SRAM_APEX_REG_675

Name: IMEM_SRAM_APEX_REG_675
Address: 675 (2A3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_ROLL_PITCH[31:24]	Gyroscope integration error related to bias precision. Higher value increases accel roll/pitch correction in steady state. Unit: LSB Default: 20

18.152 IMEM_SRAM_APEX_REG_676

Name: IMEM_SRAM_APEX_REG_676
Address: 676 (2A4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[7:0]	Gyroscope integration error related to bias precision. Higher value increases compass yaw correction in steady state. Unit: LSB Default : 20

18.153 IMEM_SRAM_APEX_REG_677

Name: IMEM_SRAM_APEX_REG_677
Address: 677 (2A5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[15:8]	Gyroscope integration error related to bias precision. Higher value increases compass yaw correction in steady state. Unit: LSB Default : 20

18.154 IMEM_SRAM_APEX_REG_678

Name: IMEM_SRAM_APEX_REG_678
Address: 678 (2A6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[23:16]	Gyroscope integration error related to bias precision. Higher value increases compass yaw correction in steady state. Unit: LSB Default : 20

18.155 IMEM_SRAM_APEX_REG_679

Name: IMEM_SRAM_APEX_REG_679
Address: 679 (2A7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_LOW_SPEED_DRIFT_YAW[31:24]	Gyroscope integration error related to bias precision. Higher value increases compass yaw correction in steady state. Unit: LSB Default : 20

18.156 IMEM_SRAM_APEX_REG_684

Name: IMEM_SRAM_APEX_REG_684
Address: 684 (2ACh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_PLL_CLOCK_VARIATION[7:0]	Error on the clock in same format as reg SW_PLL1_TRIM. Calculated as (actual_clk - target_clk) / target_clk * (2^7 - 1) / 5 * 100. Default: 0

18.157 IMEM_SRAM_APEX_REG_685

Name: IMEM_SRAM_APEX_REG_685
Address: 685 (2ADh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STATIONARY_ANGLE_ENABLE[7:0]	Enable/disable stop integration of stationary angle. Default: 0

18.158 IMEM_SRAM_APEX_REG_686

Name: IMEM_SRAM_APEX_REG_686
Address: 686 (2AEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_RUN_SPHERICAL[7:0]	Enable fusion or only calibration: 0: Run only calibration steps 1: Run also fusion/spherical steps Default: 1

18.159 IMEM_SRAM_APEX_REG_1184

Name: IMEM_SRAM_APEX_REG_1184
Address: 1184 (4A0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_DT_US[7:0]	Gyro ODR corrected with PLL clock correction. Unit: µs Default: 20000

18.160 IMEM_SRAM_APEX_REG_1185

Name: IMEM_SRAM_APEX_REG_1185
Address: 1185 (4A1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_DT_US[15:8]	Gyro ODR corrected with PLL clock correction. Unit: µs Default: 20000

18.161 IMEM_SRAM_APEX_REG_1186

Name: IMEM_SRAM_APEX_REG_1186
Address: 1186 (4A2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_DT_US[23:16]	Gyro ODR corrected with PLL clock correction. Unit: µs Default: 20000

18.162 IMEM_SRAM_APEX_REG_1187

Name: IMEM_SRAM_APEX_REG_1187
Address: 1187 (4A3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_DT_US[31:24]	Gyro ODR corrected with PLL clock correction. Unit: µs Default: 20000

18.163 IMEM_SRAM_APEX_REG_1192

Name: IMEM_SRAM_APEX_REG_1192
Address: 1192 (4A8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_DT_US[7:0]	Mag ODR as configured for magnetometer-based fusion. Unit: µs Default: 20000

18.164 IMEM_SRAM_APEX_REG_1193

Name: IMEM_SRAM_APEX_REG_1193
Address: 1193 (4A9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_DT_US[15:8]	Mag ODR as configured for magnetometer-based fusion. Unit: µs Default: 20000

18.165 IMEM_SRAM_APEX_REG_1194

Name: IMEM_SRAM_APEX_REG_1194
Address: 1194 (4AAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_DT_US[23:16]	Mag ODR as configured for magnetometer-based fusion. Unit: µs Default: 20000

18.166 IMEM_SRAM_APEX_REG_1195

Name: IMEM_SRAM_APEX_REG_1195
Address: 1195 (4ABh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_DT_US [31:24]	Mag ODR as configured for magnetometer-based fusion. Unit: µs Default: 20000

18.167 IMEM_SRAM_APEX_REG_1208

Name: IMEM_SRAM_APEX_REG_1208
Address: 1208 (4B8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[7:0]	Magnetometer measurement covariance. Unit: µT^2 s32q16 Default: 65536 (so 1.0µT^2)

18.168 IMEM_SRAM_APEX_REG_1209

Name: IMEM_SRAM_APEX_REG_1209
Address: 1209 (4B9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[15:8]	Magnetometer measurement covariance. Unit: µT^2 s32q16 Default: 65536 (so 1.0µT^2)

18.169 IMEM_SRAM_APEX_REG_1210

Name: IMEM_SRAM_APEX_REG_1210
Address: 1210 (4BAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[23:16]	Magnetometer measurement covariance. Unit: µT^2 s32q16 Default: 65536 (so 1.0µT^2)

18.170 IMEM_SRAM_APEX_REG_1211

Name: IMEM_SRAM_APEX_REG_1211
Address: 1211 (4BBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_MAG[31:24]	Magnetometer measurement covariance. Unit: µT^2 s32q16 Default: 65536 (so 1.0µT^2)

18.171 IMEM_SRAM_APEX_REG_1212

Name: IMEM_SRAM_APEX_REG_1212
Address: 1212 (4BCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[7:0]	Magnetometer anomalies rejection. Unit: µT^2 s32q30 Default: 1073741824 (so 1.0µT^2)

18.172 IMEM_SRAM_APEX_REG_1213

Name: IMEM_SRAM_APEX_REG_1213
Address: 1213 (4BDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[15:8]	Magnetometer anomalies rejection. Unit: µT^2 s32q30 Default: 1073741824 (so 1.0µT^2)

18.173 IMEM_SRAM_APEX_REG_1214

Name: IMEM_SRAM_APEX_REG_1214
Address: 1214 (4BEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[23:16]	Magnetometer anomalies rejection. Unit: µT^2 s32q30 Default: 1073741824 (so 1.0µT^2)

18.174 IMEM_SRAM_APEX_REG_1215

Name: IMEM_SRAM_APEX_REG_1215
Address: 1215 (4BFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MAG_ANOMALY_REJECTION[31:24]	Magnetometer anomalies rejection. Unit: µT^2 s32q30 Default: 1073741824 (so 1.0µT^2)

18.175 IMEM_SRAM_APEX_REG_1220

Name: IMEM_SRAM_APEX_REG_1220
Address: 1220 (4C4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_LOCK_ACC[7:0]	Threshold of steady accelerometer. Default: -1 (Disable the Lock mode feature)

18.176 IMEM_SRAM_APEX_REG_1221

Name: IMEM_SRAM_APEX_REG_1221
Address: 1221 (4C5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_LOCK_ACC[15:8]	Threshold of steady accelerometer. Default: -1 (Disable the Lock mode feature)

18.177 IMEM_SRAM_APEX_REG_1222

Name: IMEM_SRAM_APEX_REG_1222
Address: 1222 (4C6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_LOCK_ACC[23:16]	Threshold of steady accelerometer. Default: -1 (Disable the Lock mode feature)

18.178 IMEM_SRAM_APEX_REG_1223

Name: IMEM_SRAM_APEX_REG_1223
Address: 1223 (4C7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_LOCK_ACC[31:24]	Threshold of steady accelerometer. Default: -1 (Disable the Lock mode feature)

18.179 IMEM_SRAM_APEX_REG_1232

Name: IMEM_SRAM_APEX_REG_1232
Address: 1232 (4D0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[7:0]	Parameter to stop yaw error correction when value to correct is lower than threshold. Unit: rad s32q30 Default: -1 (deactivated feature)

18.180 IMEM_SRAM_APEX_REG_1233

Name: IMEM_SRAM_APEX_REG_1233
Address: 1233 (4D1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[15:8]	Parameter to stop yaw error correction when value to correct is lower than threshold. Unit: rad s32q30 Default: -1 (deactivated feature)

18.181 IMEM_SRAM_APEX_REG_1234

Name: IMEM_SRAM_APEX_REG_1234
Address: 1234 (4D2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[23:16]	Parameter to stop yaw error correction when value to correct is lower than threshold. Unit: rad s32q30 Default: -1 (deactivated feature)

18.182 IMEM_SRAM_APEX_REG_1235

Name: IMEM_SRAM_APEX_REG_1235
Address: 1235 (4D3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_STOP_CONVERGENCE[31:24]	Parameter to stop yaw error correction when value to correct is lower than threshold. Unit: rad s32q30 Default: -1 (deactivated feature)

18.183 IMEM_SRAM_APEX_REG_1236

Name: IMEM_SRAM_APEX_REG_1236
Address: 1236 (4D4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[7:0]	Parameter to control yaw error correction speed as a percentage of the gyro speed. Unit: percentage in s32q15 Default: -1 (deactivated feature)

18.184 IMEM_SRAM_APEX_REG_1237

Name: IMEM_SRAM_APEX_REG_1237
Address: 1237 (4D5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[15:8]	Parameter to control yaw error correction speed as a percentage of the gyro speed. Unit: percentage in s32q15 Default: -1 (deactivated feature)

18.185 IMEM_SRAM_APEX_REG_1238

Name: IMEM_SRAM_APEX_REG_1238
Address: 1238 (4D6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[23:16]	Parameter to control yaw error correction speed as a percentage of the gyro speed. Unit: percentage in s32q15 Default: -1 (deactivated feature)

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18.186 IMEM_SRAM_APEX_REG_1239

Name: IMEM_SRAM_APEX_REG_1239
Address: 1239 (4D7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_THRESH_YAW_SMOOTH_CONVERGENCE[31:24]	Parameter to control yaw error correction speed as a percentage of the gyro speed. Unit: percentage in s32q15 Default: -1 (deactivated feature)

18.187 IMEM_SRAM_APEX_REG_1240

Name: IMEM_SRAM_APEX_REG_1240
Address: 1240 (4D8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[7:0]	Accelerometer measurement covariance. Unit: g^2 s32q15 Default: 32768 (so 0.5g^2)

18.188 IMEM_SRAM_APEX_REG_1241

Name: IMEM_SRAM_APEX_REG_1241
Address: 1241 (4D9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[15:8]	Accelerometer measurement covariance. Unit: g^2 s32q15 Default: 32768 (so 0.5g^2)

18.189 IMEM_SRAM_APEX_REG_1242

Name: IMEM_SRAM_APEX_REG_1242
Address: 1242 (4DAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[23:16]	Accelerometer measurement covariance. Unit: g^2 s32q15 Default: 32768 (so 0.5g^2)

18.190 IMEM_SRAM_APEX_REG_1243

Name: IMEM_SRAM_APEX_REG_1243
Address: 1243 (4DBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_MEASUREMENT_COVARIANCE_ACC[31:24]	Accelerometer measurement covariance. Unit: g^2 s32q15 Default: 32768 (so 0.5g^2)

18.191 IMEM_SRAM_APEX_REG_1268

Name: IMEM_SRAM_APEX_REG_1268
Address: 1268 (4F4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_ACCELERATION_REJECTION[7:0]	Linear acceleration rejection. Unit: m/s^2 s32q30 Range: [0 - 1073741824] Default: 1073741824 (so 1.0, being maximum rejection)

18.192 IMEM_SRAM_APEX_REG_1269

Name: IMEM_SRAM_APEX_REG_1269
Address: 1269 (4F5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_ACCELERATION_REJECTION[15:8]	Linear acceleration rejection. Unit: m/s^2 s32q30 Range: [0 - 1073741824] Default: 1073741824 (so 1.0, being maximum rejection)

18.193 IMEM_SRAM_APEX_REG_1270

Name: IMEM_SRAM_APEX_REG_1270
Address: 1270 (4F6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_ACCELERATION_REJECTION[23:16]	Linear acceleration rejection. Unit: m/s^2 s32q30 Range: [0 - 1073741824] Default: 1073741824 (so 1.0, being maximum rejection)

18.194 IMEM_SRAM_APEX_REG_1271

Name: IMEM_SRAM_APEX_REG_1271
Address: 1271 (4F7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_ACCELERATION_REJECTION[31:24]	Linear acceleration rejection. Unit: m/s^2 s32q30 Range: [0 - 1073741824] Default: 1073741824 (so 1.0, being maximum rejection)

18.195 IMEM_SRAM_APEX_REG_1272

Name: IMEM_SRAM_APEX_REG_1272
Address: 1272 (4F8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[7:0]	Percentage of error (covering gyroscope sensitivity, timestamp and quantization) on gyroscope integration. Unit: LSB with 2^15 LSB = 1% error Default: 262144 (so 8% error)

18.196 IMEM_SRAM_APEX_REG_1273

Name: IMEM_SRAM_APEX_REG_1273
Address: 1273 (4F9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[15:8]	Percentage of error (covering gyroscope sensitivity, timestamp and quantization) on gyroscope integration. Unit: LSB with 2^15 LSB = 1% error Default: 262144 (so 8% error)

18.197 IMEM_SRAM_APEX_REG_1274

Name: IMEM_SRAM_APEX_REG_1274
Address: 1274 (4FAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[23:16]	Percentage of error (covering gyroscope sensitivity, timestamp and quantization) on gyroscope integration. Unit: LSB with 2^15 LSB = 1% error Default: 262144 (so 8% error)

18.198 IMEM_SRAM_APEX_REG_1275

Name: IMEM_SRAM_APEX_REG_1275
Address: 1275 (4FBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_FUS_HIGH_SPEED_DRIFT[31:24]	Percentage of error (covering gyroscope sensitivity, timestamp and quantization) on gyroscope integration. Unit: LSB with 2^15 LSB = 1% error Default: 262144 (so 8% error)

18.199 IMEM_SRAM_APEX_REG_1468

Name: IMEM_SRAM_APEX_REG_1468
Address: 1468 (5BCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_ACCURACY[7:0]	Gyroscope accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.200 IMEM_SRAM_APEX_REG_1469

Name: IMEM_SRAM_APEX_REG_1469
Address: 1469 (5BDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_ACCURACY[15:8]	Gyroscope accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.201 IMEM_SRAM_APEX_REG_1470

Name: IMEM_SRAM_APEX_REG_1470
Address: 1470 (5BEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_ACCURACY[23:16]	Gyroscope accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.202 IMEM_SRAM_APEX_REG_1471

Name: IMEM_SRAM_APEX_REG_1471
Address: 1471 (5BFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_ACCURACY[31:24]	Gyroscope accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.203 IMEM_SRAM_APEX_REG_1484

Name: IMEM_SRAM_APEX_REG_1484
Address: 1484 (5CCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[7:0]	Duration for no motion gyroscope bias calibration. Unit: µs Default value: 500000

18.204 IMEM_SRAM_APEX_REG_1485

Name: IMEM_SRAM_APEX_REG_1485
Address: 1485 (5CDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[15:8]	Duration for no motion gyroscope bias calibration. Unit: µs Default value: 500000

18.205 IMEM_SRAM_APEX_REG_1486

Name: IMEM_SRAM_APEX_REG_1486
Address: 1486 (5CEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[23:16]	Duration for no motion gyroscope bias calibration. Unit: µs Default value: 500000

18.206 IMEM_SRAM_APEX_REG_1487

Name: IMEM_SRAM_APEX_REG_1487
Address: 1487 (5CFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_STATIONARY_DURATION_US[31:24]	Duration for no motion gyroscope bias calibration. Unit: µs Default value: 500000

18.207 IMEM_SRAM_APEX_REG_1500

Name: IMEM_SRAM_APEX_REG_1500
Address: 1500 (5DCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[7:0]	Stationary detection threshold of 2nd metric for the loose bias calibration. Default value: 60000 (no unit).

18.208 IMEM_SRAM_APEX_REG_1501

Name: IMEM_SRAM_APEX_REG_1501
Address: 1501 (5DDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[15:8]	Stationary detection threshold of 2nd metric for the loose bias calibration. Default value: 60000 (no unit).

18.209 IMEM_SRAM_APEX_REG_1502

Name: IMEM_SRAM_APEX_REG_1502
Address: 1502 (5DEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[23:16]	Stationary detection threshold of 2nd metric for the loose bias calibration. Default value: 60000 (no unit).

18.210 IMEM_SRAM_APEX_REG_1503

Name: IMEM_SRAM_APEX_REG_1503
Address: 1503 (5DFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC2[31:24]	Stationary detection threshold of 2nd metric for the loose bias calibration. Default value: 60000 (no unit).

18.211 IMEM_SRAM_APEX_REG_1504

Name: IMEM_SRAM_APEX_REG_1504
Address: 1504 (5E0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_BIAS_REJECT_TH[7:0]	Gyro bias rejection threshold above which device is considered as moving. Threshold is compared against absolute value of delta between current estimated gyro bias and last estimated gyro bias in an analysis window. Unit: 2000dps = 2^30 Default value: 3650722 (so 6.8dps)

18.212 IMEM_SRAM_APEX_REG_1505

Name: IMEM_SRAM_APEX_REG_1505
Address: 1505 (5E1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_BIAS_REJECT_TH[15:8]	Gyro bias rejection threshold above which device is considered as moving. Threshold is compared against absolute value of delta between current estimated gyro bias and last estimated gyro bias in an analysis window. Unit: 2000dps = 2^30 Default value: 3650722 (so 6.8dps)

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18.213 IMEM_SRAM_APEX_REG_1506

Name: IMEM_SRAM_APEX_REG_1506
Address: 1506 (5E2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_BIAS_REJECT_TH[23:16]	Gyro bias rejection threshold above which device is considered as moving. Threshold is compared against absolute value of delta between current estimated gyro bias and last estimated gyro bias in an analysis window. Unit: 2000dps = 2^30 Default value: 3650722 (so 6.8dps)

18.214 IMEM_SRAM_APEX_REG_1507

Name: IMEM_SRAM_APEX_REG_1507
Address: 1507 (5E3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GYR_BIAS_REJECT_TH[31:24]	Gyro bias rejection threshold above which device is considered as moving. Threshold is compared against absolute value of delta between current estimated gyro bias and last estimated gyro bias in an analysis window. Unit: 2000dps = 2^30 Default value: 3650722 (so 6.8dps)

18.215 IMEM_SRAM_APEX_REG_1516

Name: IMEM_SRAM_APEX_REG_1516
Address: 1516 (5ECh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[7:0]	Stationary detection threshold of 1st metric for the loose bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 1200 (so 2.28dps)

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18.216 IMEM_SRAM_APEX_REG_1517

Name: IMEM_SRAM_APEX_REG_1517
Address: 1517 (5EDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[15:8]	Stationary detection threshold of 1st metric for the loose bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 1200 (so 2.28dps)

18.217 IMEM_SRAM_APEX_REG_1518

Name: IMEM_SRAM_APEX_REG_1518
Address: 1518 (5EEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[23:16]	Stationary detection threshold of 1st metric for the loose bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 1200 (so 2.28dps)

18.218 IMEM_SRAM_APEX_REG_1519

Name: IMEM_SRAM_APEX_REG_1519
Address: 1519 (5EFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_THRESHOLD_METRIC1[31:24]	Stationary detection threshold of 1st metric for the loose bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 1200 (so 2.28dps)

18.219 IMEM_SRAM_APEX_REG_1696

Name: IMEM_SRAM_APEX_REG_1696
Address: 1696 (6A0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[7:0]	Previously stored temperature when gyro bias was estimated. Unit: degree C in s32q16

18.220 IMEM_SRAM_APEX_REG_1697

Name: IMEM_SRAM_APEX_REG_1697
Address: 1697 (6A1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[15:8]	Previously stored temperature when gyro bias was estimated. Unit: degree C in s32q16

18.221 IMEM_SRAM_APEX_REG_1698

Name: IMEM_SRAM_APEX_REG_1698
Address: 1698 (6A2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[23:16]	Previously stored temperature when gyro bias was estimated. Unit: degree C in s32q16

18.222 IMEM_SRAM_APEX_REG_1699

Name: IMEM_SRAM_APEX_REG_1699
Address: 1699 (6A3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_TEMPERATURE_DEG_Q16[31:24]	Previously stored temperature when gyro bias was estimated. Unit: degree C in s32q16

18.223 IMEM_SRAM_APEX_REG_1712

Name: IMEM_SRAM_APEX_REG_1712
Address: 1712 (6B0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[7:0]	Square of sin on angle threshold to reject gyroscope calibration. Unit: (sin(theta)2)*225 Default: 4318 (so 0.65 degree)

18.224 IMEM_SRAM_APEX_REG_1713

Name: IMEM_SRAM_APEX_REG_1713
Address: 1713 (6B1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[15:8]	Square of sin on angle threshold to reject gyroscope calibration. Unit: (sin(theta)2)*225 Default: 4318 (so 0.65 degree)

18.225 IMEM_SRAM_APEX_REG_1714

Name: IMEM_SRAM_APEX_REG_1714
Address: 1714 (6B2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[23:16]	Square of sin on angle threshold to reject gyroscope calibration. Unit: (sin(theta)2)*225 Default: 4318 (so 0.65 degree)

18.226 IMEM_SRAM_APEX_REG_1715

Name: IMEM_SRAM_APEX_REG_1715
Address: 1715 (6B3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_SQUARE_SIN_ANGLE_MOTION_DETECT_TH[31:24]	Square of sin on angle threshold to reject gyroscope calibration. Unit: (sin(theta)2)*225 Default: 4318 (so 0.65 degree)

18.227 IMEM_SRAM_APEX_REG_1716

Name: IMEM_SRAM_APEX_REG_1716
Address: 1716 (6B4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[7:0]	Accelerometer filtering mean value. Unit: sample number in log2 Default: 5 (so 32 samples)

18.228 IMEM_SRAM_APEX_REG_1717

Name: IMEM_SRAM_APEX_REG_1717
Address: 1717 (6B5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[15:8]	Accelerometer filtering mean value. Unit: sample number in log2 Default: 5 (so 32 samples)

18.229 IMEM_SRAM_APEX_REG_1718

Name: IMEM_SRAM_APEX_REG_1718
Address: 1718 (6B6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[23:16]	Accelerometer filtering mean value. Unit: sample number in log2 Default: 5 (so 32 samples)

18.230 IMEM_SRAM_APEX_REG_1719

Name: IMEM_SRAM_APEX_REG_1719
Address: 1719 (6B7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_ACC_FILTERING_NPOINTS_LOG2[31:24]	Accelerometer filtering mean value. Unit: sample number in log2 Default: 5 (so 32 samples)

18.231 IMEM_SRAM_APEX_REG_1720

Name: IMEM_SRAM_APEX_REG_1720
Address: 1720 (6B8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[7:0]	Stationary detection threshold of 1st metric for strict bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 300 (so 0.57dps)

18.232 IMEM_SRAM_APEX_REG_1721

Name: IMEM_SRAM_APEX_REG_1721
Address: 1721 (6B9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[15:8]	Stationary detection threshold of 1st metric for strict bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 300 (so 0.57dps)

18.233 IMEM_SRAM_APEX_REG_1722

Name: IMEM_SRAM_APEX_REG_1722
Address: 1722 (6BAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[23:16]	Stationary detection threshold of 1st metric for strict bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 300 (so 0.57dps)

18.234 IMEM_SRAM_APEX_REG_1723

Name: IMEM_SRAM_APEX_REG_1723
Address: 1723 (6BBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC1[31:24]	Stationary detection threshold of 1st metric for strict bias calibration. Threshold is compared against absolute value of delta between current gyro value and last gyro value in an analysis window. Unit: 2000dps = 2^20 Default value: 300 (so 0.57dps)

18.235 IMEM_SRAM_APEX_REG_1724

Name: IMEM_SRAM_APEX_REG_1724
Address: 1724 (6BCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[7:0]	Stationary detection threshold of 2nd metric for the strict bias calibration. Default value: 400

18.236 IMEM_SRAM_APEX_REG_1725

Name: IMEM_SRAM_APEX_REG_1725
Address: 1725 (6BDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[15:8]	Stationary detection threshold of 2nd metric for the strict bias calibration. Default value: 400

18.237 IMEM_SRAM_APEX_REG_1726

Name: IMEM_SRAM_APEX_REG_1726
Address: 1726 (6BEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[23:16]	Stationary detection threshold of 2nd metric for the strict bias calibration. Default value: 400

18.238 IMEM_SRAM_APEX_REG_1727

Name: IMEM_SRAM_APEX_REG_1727
Address: 1727 (6BFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_STRICT_GYR_CAL_THRESHOLD_METRIC2[31:24]	Stationary detection threshold of 2nd metric for the strict bias calibration. Default value: 400

18.239 IMEM_SRAM_APEX_REG_1728

Name: IMEM_SRAM_APEX_REG_1728
Address: 1728 (6C0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TIMER[7:0]	Validity timer of the strict bias in sample number. Default: 1440000 (so 8 hours at 50Hz)

18.240 IMEM_SRAM_APEX_REG_1729

Name: IMEM_SRAM_APEX_REG_1729
Address: 1729 (6C1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TIMER[15:8]	Validity timer of the strict bias in sample number. Default: 1440000 (so 8 hours at 50Hz)

18.241 IMEM_SRAM_APEX_REG_1730

Name: IMEM_SRAM_APEX_REG_1730
Address: 1730 (6C2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TIMER[23:16]	Validity timer of the strict bias in sample number. Default: 1440000 (so 8 hours at 50Hz)

18.242 IMEM_SRAM_APEX_REG_1731

Name: IMEM_SRAM_APEX_REG_1731
Address: 1731 (6C3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TIMER[31:24]	Validity timer of the strict bias in sample number. Default: 1440000 (so 8 hours at 50Hz)

18.243 IMEM_SRAM_APEX_REG_1732

Name: IMEM_SRAM_APEX_REG_1732
Address: 1732 (6C4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[7:0]	Validity temperature variation of the strict bias. Unit: degree C s32q16 Default: 983040 (so 15 degree C)

18.244 IMEM_SRAM_APEX_REG_1733

Name: IMEM_SRAM_APEX_REG_1733
Address: 1733 (6C5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[15:8]	Validity temperature variation of the strict bias. Unit: degree C s32q16 Default: 983040 (so 15 degree C)

18.245 IMEM_SRAM_APEX_REG_1734

Name: IMEM_SRAM_APEX_REG_1734
Address: 1734 (6C6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[23:16]	Validity temperature variation of the strict bias. Unit: degree C s32q16 Default: 983040 (so 15 degree C)

18.246 IMEM_SRAM_APEX_REG_1735

Name: IMEM_SRAM_APEX_REG_1735
Address: 1735 (6C7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_GOLDEN_BIAS_TEMPERATURE_VALIDITY[31:24]	Validity temperature variation of the strict bias. Unit: degree C s32q16 Default: 983040 (so 15 degree C)

18.247 IMEM_SRAM_APEX_REG_1736

Name: IMEM_SRAM_APEX_REG_1736
Address: 1736 (6C8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[7:0]	Gyroscope calibration number of samples used to estimate metric1 and metric2, and minimum gyroscope calibration duration. Unit: number of samples in log2 Range: [6 - 8] Default: 7 (so 2^7 = 128 samples)

18.248 IMEM_SRAM_APEX_REG_1737

Name: IMEM_SRAM_APEX_REG_1737
Address: 1737 (6C9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[15:8]	Gyroscope calibration number of samples used to estimate metric1 and metric2, and minimum gyroscope calibration duration. Unit: number of samples in log2 Range: [6 - 8] Default: 7 (so 2^7 = 128 samples)

18.249 IMEM_SRAM_APEX_REG_1738

Name: IMEM_SRAM_APEX_REG_1738
Address: 1738 (6CAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[23:16]	Gyroscope calibration number of samples used to estimate metric1 and metric2, and minimum gyroscope calibration duration. Unit: number of samples in log2 Range: [6 - 8]

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		Default: 7 (so 2^7 = 128 samples)

18.250 IMEM_SRAM_APEX_REG_1739

Name: IMEM_SRAM_APEX_REG_1739
Address: 1739 (6CBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_LOOSE_GYR_CAL_SAMPLE_NUM_LOG2[31:24]	Gyroscope calibration number of samples used to estimate metric1 and metric2, and minimum gyroscope calibration duration. Unit: number of samples in log2 Range: [6 - 8] Default: 7 (so 2^7 = 128 samples)

18.251 IMEM_SRAM_APEX_REG_1740

Name: IMEM_SRAM_APEX_REG_1740
Address: 1740 (6CCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[7:0]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.252 IMEM_SRAM_APEX_REG_1741

Name: IMEM_SRAM_APEX_REG_1741
Address: 1741 (6CDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[15:8]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.253 IMEM_SRAM_APEX_REG_1742

Name: IMEM_SRAM_APEX_REG_1742
Address: 1742 (6CEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[23:16]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.254 IMEM_SRAM_APEX_REG_1743

Name: IMEM_SRAM_APEX_REG_1743
Address: 1743 (6CFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[31:24]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.255 IMEM_SRAM_APEX_REG_1744

Name: IMEM_SRAM_APEX_REG_1744
Address: 1744 (6D0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[39:32]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.256 IMEM_SRAM_APEX_REG_1745

Name: IMEM_SRAM_APEX_REG_1745
Address: 1745 (6D1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[47:40]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.257 IMEM_SRAM_APEX_REG_1746

Name: IMEM_SRAM_APEX_REG_1746
Address: 1746 (6D2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[55:48]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.258 IMEM_SRAM_APEX_REG_1747

Name: IMEM_SRAM_APEX_REG_1747
Address: 1747 (6D3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[63:56]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.259 IMEM_SRAM_APEX_REG_1748

Name: IMEM_SRAM_APEX_REG_1748
Address: 1748 (6D4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[71:64]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.260 IMEM_SRAM_APEX_REG_1749

Name: IMEM_SRAM_APEX_REG_1749
Address: 1749 (6D5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[79:72]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.261 IMEM_SRAM_APEX_REG_1750

Name: IMEM_SRAM_APEX_REG_1750
Address: 1750 (6D6h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[87:80]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.262 IMEM_SRAM_APEX_REG_1751

Name: IMEM_SRAM_APEX_REG_1751
Address: 1751 (6D7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_GYR_BIAS_DPS_Q12[95:88]	Previous gyroscope bias to start with (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.263 IMEM_SRAM_APEX_REG_1900

Name: IMEM_SRAM_APEX_REG_1900
Address: 1900 (76Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY_COVARIANCE[7:0]	Magnetometer maximum covariance inherited from new mag accuracy to be applied. Range: 2499 for accuracy 3, 4999 for accuracy 2, 9999 for accuracy 1, 500000 for accuracy 0 Default: 500000

18.264 IMEM_SRAM_APEX_REG_1901

Name: IMEM_SRAM_APEX_REG_1901
Address: 1901 (76Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY_COVARIANCE[15:8]	Magnetometer maximum covariance inherited from new mag accuracy to be applied. Range: 2499 for accuracy 3, 4999 for accuracy 2, 9999 for accuracy 1, 500000 for accuracy 0 Default: 500000

18.265 IMEM_SRAM_APEX_REG_1902

Name: IMEM_SRAM_APEX_REG_1902
Address: 1902 (76Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY_COVARIANCE[23:16]	Magnetometer maximum covariance inherited from new mag accuracy to be applied. Range: 2499 for accuracy 3, 4999 for accuracy 2, 9999 for accuracy 1, 500000 for accuracy 0

		Default: 500000

18.266 IMEM_SRAM_APEX_REG_1903

Name: IMEM_SRAM_APEX_REG_1903
Address: 1903 (76Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY_COVARIANCE[31:24]	Magnetometer maximum covariance inherited from new mag accuracy to be applied. Range: 2499 for accuracy 3, 4999 for accuracy 2, 9999 for accuracy 1, 500000 for accuracy 0 Default: 500000

18.267 IMEM_SRAM_APEX_REG_1904

Name: IMEM_SRAM_APEX_REG_1904
Address: 1904 (770h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY[7:0]	Magnetometer accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.268 IMEM_SRAM_APEX_REG_1905

Name: IMEM_SRAM_APEX_REG_1905
Address: 1905 (771h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY[15:8]	Magnetometer accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.269 IMEM_SRAM_APEX_REG_1906

Name: IMEM_SRAM_APEX_REG_1906
Address: 1906 (772h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY[23:16]	Magnetometer accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.270 IMEM_SRAM_APEX_REG_1907

Name: IMEM_SRAM_APEX_REG_1907
Address: 1907 (773h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_ACCURACY[31:24]	Magnetometer accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.271 IMEM_SRAM_APEX_REG_1908

Name: IMEM_SRAM_APEX_REG_1908
Address: 1908 (774h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[7:0]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.272 IMEM_SRAM_APEX_REG_1909

Name: IMEM_SRAM_APEX_REG_1909
Address: 1909 (775h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[15:8]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.273 IMEM_SRAM_APEX_REG_1910

Name: IMEM_SRAM_APEX_REG_1910
Address: 1910 (776h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[23:16]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.274 IMEM_SRAM_APEX_REG_1911

Name: IMEM_SRAM_APEX_REG_1911
Address: 1911 (777h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[31:24]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.275 IMEM_SRAM_APEX_REG_1912

Name: IMEM_SRAM_APEX_REG_1912
Address: 1912 (778h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[39:32]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.276 IMEM_SRAM_APEX_REG_1913

Name: IMEM_SRAM_APEX_REG_1913
Address: 1913 (779h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[47:40]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.277 IMEM_SRAM_APEX_REG_1914

Name: IMEM_SRAM_APEX_REG_1914
Address: 1914 (77Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[55:48]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.278 IMEM_SRAM_APEX_REG_1915

Name: IMEM_SRAM_APEX_REG_1915
Address: 1915 (77Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[63:56]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.279 IMEM_SRAM_APEX_REG_1916

Name: IMEM_SRAM_APEX_REG_1916
Address: 1916 (77Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[71:64]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.280 IMEM_SRAM_APEX_REG_1917

Name: IMEM_SRAM_APEX_REG_1917
Address: 1917 (77Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[79:72]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.281 IMEM_SRAM_APEX_REG_1918

Name: IMEM_SRAM_APEX_REG_1918
Address: 1918 (77Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[87:80]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.282 IMEM_SRAM_APEX_REG_1919

Name: IMEM_SRAM_APEX_REG_1919
Address: 1919 (77Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_MAG_BIAS_UT_Q16[95:88]	Magnetometer bias to start with (one value per axis). Unit: dps in s32q16 Default: 0;0;0

18.283 IMEM_SRAM_APEX_REG_2072

Name: IMEM_SRAM_APEX_REG_2072
Address: 2072 (818h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAGCAL_DT_US[7:0]	Mag ODR as configured for magnetometer calibration. Must match gaf_config_mag_dt_us value at any time. Unit: µs Default: 20000

18.284 IMEM_SRAM_APEX_REG_2073

Name: IMEM_SRAM_APEX_REG_2073
Address: 2073 (819h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAGCAL_DT_US[15:8]	Mag ODR as configured for magnetometer calibration. Must match gaf_config_mag_dt_us value at any time. Unit: µs Default: 20000

18.285 IMEM_SRAM_APEX_REG_2074

Name: IMEM_SRAM_APEX_REG_2074
Address: 2074 (81Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAGCAL_DT_US[23:16]	Mag ODR as configured for magnetometer calibration. Must match gaf_config_mag_dt_us value at any time. Unit: µs Default: 20000

18.286 IMEM_SRAM_APEX_REG_2075

Name: IMEM_SRAM_APEX_REG_2075
Address: 2075 (81Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAGCAL_DT_US[31:24]	Mag ODR as configured for magnetometer calibration. Must match gaf_config_mag_dt_us value at any time. Unit: µs Default: 20000

18.287 IMEM_SRAM_APEX_REG_2080

Name: IMEM_SRAM_APEX_REG_2080
Address: 2080 (820h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[7:0]	Huge disturbance threshold to reset the algorithm. Unit: µT in s32q11 Default: 409600 (200 µT)

18.288 IMEM_SRAM_APEX_REG_2081

Name: IMEM_SRAM_APEX_REG_2081
Address: 2081 (821h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[15:8]	Huge disturbance threshold to reset the algorithm. Unit: µT in s32q11 Default: 409600 (200 µT)

18.289 IMEM_SRAM_APEX_REG_2082

Name: IMEM_SRAM_APEX_REG_2082
Address: 2082 (822h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[23:16]	Huge disturbance threshold to reset the algorithm. Unit: µT in s32q11 Default: 409600 (200 µT)

18.290 IMEM_SRAM_APEX_REG_2083

Name: IMEM_SRAM_APEX_REG_2083
Address: 2083 (823h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_HUGE_DISTURBANCE[31:24]	Huge disturbance threshold to reset the algorithm. Unit: µT in s32q11 Default: 409600 (200 µT)

18.291 IMEM_SRAM_APEX_REG_2084

Name: IMEM_SRAM_APEX_REG_2084
Address: 2084 (824h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[7:0]	Difference between current radius and measurement to switch to disturbed state. Unit: µT in s32q11 Default: 30720 (15 µT)

18.292 IMEM_SRAM_APEX_REG_2085

Name: IMEM_SRAM_APEX_REG_2085
Address: 2085 (825h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[15:8]	Difference between current radius and measurement to switch to disturbed state. Unit: µT in s32q11 Default: 30720 (15 µT)

18.293 IMEM_SRAM_APEX_REG_2086

Name: IMEM_SRAM_APEX_REG_2086
Address: 2086 (826h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[23:16]	Difference between current radius and measurement to switch to disturbed state. Unit: µT in s32q11 Default: 30720 (15 µT)

18.294 IMEM_SRAM_APEX_REG_2087

Name: IMEM_SRAM_APEX_REG_2087
Address: 2087 (827h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_ANOMALY_RADIUS[31:24]	Difference between current radius and measurement to switch to disturbed state. Unit: µT in s32q11 Default: 30720 (15 µT)

18.295 IMEM_SRAM_APEX_REG_2088

Name: IMEM_SRAM_APEX_REG_2088
Address: 2088 (828h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_ANGLE[7:0]	Minimum angular variation between 2 consecutive measurements (using gyro). Unit: s32q30 Default: 1050277989 (cos(12deg))

18.296 IMEM_SRAM_APEX_REG_2089

Name: IMEM_SRAM_APEX_REG_2089
Address: 2089 (829h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_ANGLE[15:8]	Minimum angular variation between 2 consecutive measurements (using gyro). Unit: s32q30 Default: 1050277989 (cos(12deg))

18.297 IMEM_SRAM_APEX_REG_2090

Name: IMEM_SRAM_APEX_REG_2090
Address: 2090 (82Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_ANGLE[23:16]	Minimum angular variation between 2 consecutive measurements (using gyro). Unit: s32q30 Default: 1050277989 (cos(12deg))

18.298 IMEM_SRAM_APEX_REG_2091

Name: IMEM_SRAM_APEX_REG_2091
Address: 2091 (82Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_ANGLE[31:24]	Minimum angular variation between 2 consecutive measurements (using gyro). Unit: s32q30 Default: 1050277989 (cos(12deg))

18.299 IMEM_SRAM_APEX_REG_2092

Name: IMEM_SRAM_APEX_REG_2092
Address: 2092 (82Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[7:0]	Minimum distance variation between 2 consecutive measurements (using gyro). Unit: µT s32q11 Default: 10240 (5µT)

18.300 IMEM_SRAM_APEX_REG_2093

Name: IMEM_SRAM_APEX_REG_2093
Address: 2093 (82Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[15:8]	Minimum distance variation between 2 consecutive measurements (using gyro). Unit: µT s32q11 Default: 10240 (5µT)

18.301 IMEM_SRAM_APEX_REG_2094

Name: IMEM_SRAM_APEX_REG_2094
Address: 2094 (82Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[23:16]	Minimum distance variation between 2 consecutive measurements (using gyro). Unit: µT s32q11 Default: 10240 (5µT)

18.302 IMEM_SRAM_APEX_REG_2095

Name: IMEM_SRAM_APEX_REG_2095
Address: 2095 (82Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_GYRO[31:24]	Minimum distance variation between 2 consecutive measurements (using gyro). Unit: µT s32q11 Default: 10240 (5µT)

18.303 IMEM_SRAM_APEX_REG_2096

Name: IMEM_SRAM_APEX_REG_2096
Address: 2096 (830h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[7:0]	Minimum distance variation between 2 consecutive measurements (not using gyro). Unit: µT in s32q11 Default: 30720 (15µT)

18.304 IMEM_SRAM_APEX_REG_2097

Name: IMEM_SRAM_APEX_REG_2097
Address: 2097 (831h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[15:8]	Minimum distance variation between 2 consecutive measurements (not using gyro). Unit: µT in s32q11 Default: 30720 (15µT)

18.305 IMEM_SRAM_APEX_REG_2098

Name: IMEM_SRAM_APEX_REG_2098
Address: 2098 (832h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[23:16]	Minimum distance variation between 2 consecutive measurements (not using gyro). Unit: µT in s32q11 Default: 30720 (15µT)

18.306 IMEM_SRAM_APEX_REG_2099

Name: IMEM_SRAM_APEX_REG_2099
Address: 2099 (833h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_SELECT_DISTANCE_NOGYRO[31:24]	Minimum distance variation between 2 consecutive measurements (not using gyro). Unit: µT in s32q11 Default: 30720 (15µT)

18.307 IMEM_SRAM_APEX_REG_2100

Name: IMEM_SRAM_APEX_REG_2100
Address: 2100 (834h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_STANDALONE[7:0]	Magnetometer calibration model covariance. Default: 3

18.308 IMEM_SRAM_APEX_REG_2101

Name: IMEM_SRAM_APEX_REG_2101
Address: 2101 (835h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_STANDALONE[15:8]	Magnetometer calibration model covariance. Default: 3

18.309 IMEM_SRAM_APEX_REG_2102

Name: IMEM_SRAM_APEX_REG_2102
Address: 2102 (836h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_STANDALONE[23:16]	Magnetometer calibration model covariance. Default: 3

18.310 IMEM_SRAM_APEX_REG_2103

Name: IMEM_SRAM_APEX_REG_2103
Address: 2103 (837h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_STANDALONE[31:24]	Magnetometer calibration model covariance. Default: 3

18.311 IMEM_SRAM_APEX_REG_2104

Name: IMEM_SRAM_APEX_REG_2104
Address: 2104 (838h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_STANDALONE[7:0]	Magnetometer calibration measurement covariance. Default: 400000

18.312 IMEM_SRAM_APEX_REG_2105

Name: IMEM_SRAM_APEX_REG_2105
Address: 2105 (839h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_STANDALONE[15:8]	Magnetometer calibration measurement covariance. Default: 400000

18.313 IMEM_SRAM_APEX_REG_2106

Name: IMEM_SRAM_APEX_REG_2106
Address: 2106 (83Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_STANDALONE[23:16]	Magnetometer calibration measurement covariance. Default: 400000

18.314 IMEM_SRAM_APEX_REG_2107

Name: IMEM_SRAM_APEX_REG_2107
Address: 2107 (83Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_STANDALONE[31:24]	Magnetometer calibration measurement covariance. Default: 400000

18.315 IMEM_SRAM_APEX_REG_2108

Name: IMEM_SRAM_APEX_REG_2108
Address: 2108 (83Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_ASSISTED[7:0]	Magnetometer calibration model covariance for gyro assisted model. Default: 1

18.316 IMEM_SRAM_APEX_REG_2109

Name: IMEM_SRAM_APEX_REG_2109
Address: 2109 (83Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_ASSISTED[15:8]	Magnetometer calibration model covariance for gyro assisted model. Default: 1

18.317 IMEM_SRAM_APEX_REG_2110

Name: IMEM_SRAM_APEX_REG_2110
Address: 2110 (83Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_ASSISTED[23:16]	Magnetometer calibration model covariance for gyro assisted model. Default: 1

18.318 IMEM_SRAM_APEX_REG_2111

Name: IMEM_SRAM_APEX_REG_2111
Address: 2111 (83Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_Q0_ASSISTED[31:24]	Magnetometer calibration model covariance for gyro assisted model. Default: 1

18.319 IMEM_SRAM_APEX_REG_2112

Name: IMEM_SRAM_APEX_REG_2112
Address: 2112 (840h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_ASSISTED[7:0]	Magnetometer calibration measurement covariance for gyro assisted model. Default: 5000

18.320 IMEM_SRAM_APEX_REG_2113

Name: IMEM_SRAM_APEX_REG_2113
Address: 2113 (841h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_ASSISTED[15:8]	Magnetometer calibration measurement covariance for gyro assisted model. Default: 5000

18.321 IMEM_SRAM_APEX_REG_2114

Name: IMEM_SRAM_APEX_REG_2114
Address: 2114 (842h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_ASSISTED[23:16]	Magnetometer calibration measurement covariance for gyro assisted model. Default: 5000

18.322 IMEM_SRAM_APEX_REG_2115

Name: IMEM_SRAM_APEX_REG_2115
Address: 2115 (843h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_R0_ASSISTED[31:24]	Magnetometer calibration measurement covariance for gyro assisted model. Default: 5000

18.323 IMEM_SRAM_APEX_REG_2116

Name: IMEM_SRAM_APEX_REG_2116
Address: 2116 (844h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[7:0]	Maximum radius jump between 2 solutions. Unit: µT in s32q11 Default: 40960 (20µT)

18.324 IMEM_SRAM_APEX_REG_2117

Name: IMEM_SRAM_APEX_REG_2117
Address: 2117 (845h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[15:8]	Maximum radius jump between 2 solutions. Unit: µT in s32q11 Default: 40960 (20µT)

18.325 IMEM_SRAM_APEX_REG_2118

Name: IMEM_SRAM_APEX_REG_2118
Address: 2118 (846h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[23:16]	Maximum radius jump between 2 solutions. Unit: µT in s32q11 Default: 40960 (20µT)

18.326 IMEM_SRAM_APEX_REG_2119

Name: IMEM_SRAM_APEX_REG_2119
Address: 2119 (847h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS_JUMP[31:24]	Maximum radius jump between 2 solutions. Unit: µT in s32q11 Default: 40960 (20µT)

18.327 IMEM_SRAM_APEX_REG_2120

Name: IMEM_SRAM_APEX_REG_2120
Address: 2120 (848h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS[7:0]	Maximum field radius. Unit: µT in s32q11 Default: 256000 (125µT)

18.328 IMEM_SRAM_APEX_REG_2121

Name: IMEM_SRAM_APEX_REG_2121
Address: 2121 (849h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS[15:8]	Maximum field radius. Unit: µT in s32q11 Default: 256000 (125µT)

18.329 IMEM_SRAM_APEX_REG_2122

Name: IMEM_SRAM_APEX_REG_2122
Address: 2122 (84Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS[23:16]	Maximum field radius. Unit: µT in s32q11 Default: 256000 (125µT)

18.330 IMEM_SRAM_APEX_REG_2123

Name: IMEM_SRAM_APEX_REG_2123
Address: 2123 (84Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MAX_RADIUS[31:24]	Maximum field radius. Unit: µT in s32q11 Default: 256000 (125µT)

18.331 IMEM_SRAM_APEX_REG_2124

Name: IMEM_SRAM_APEX_REG_2124
Address: 2124 (84Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MIN_RADIUS[7:0]	Minimum field radius. Unit: µT in s32q11 Default: 36864 (18µT)

18.332 IMEM_SRAM_APEX_REG_2125

Name: IMEM_SRAM_APEX_REG_2125
Address: 2125 (84Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MIN_RADIUS[15:8]	Minimum field radius. Unit: µT in s32q11 Default: 36864 (18µT)

18.333 IMEM_SRAM_APEX_REG_2126

Name: IMEM_SRAM_APEX_REG_2126
Address: 2126 (84Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MIN_RADIUS[23:16]	Minimum field radius. Unit: µT in s32q11 Default: 36864 (18µT)

18.334 IMEM_SRAM_APEX_REG_2127

Name: IMEM_SRAM_APEX_REG_2127
Address: 2127 (84Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_THR_MIN_RADIUS[31:24]	Minimum field radius. Unit: µT in s32q11 Default: 36864 (18µT)

18.335 IMEM_SRAM_APEX_REG_2128

Name: IMEM_SRAM_APEX_REG_2128
Address: 2128 (850h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_CALIBRATION_CONDITION[7:0]	Control if we check additional condition on covariance in magnetometer calibration. Default: 1

18.336 IMEM_SRAM_APEX_REG_2129

Name: IMEM_SRAM_APEX_REG_2129
Address: 2129 (851h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_CONFIG_MAG_CALIBRATION_CONDITION[15:8]	Control if we check additional condition on covariance in magnetometer calibration. Default: 1

18.337 IMEM_SRAM_APEX_REG_2248

Name: IMEM_SRAM_APEX_REG_2248
Address: 2248 (8C8h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[7:0]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.338 IMEM_SRAM_APEX_REG_2249

Name: IMEM_SRAM_APEX_REG_2249
Address: 2249 (8C9h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[15:8]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.339 IMEM_SRAM_APEX_REG_2250

Name: IMEM_SRAM_APEX_REG_2250
Address: 2250 (8CAh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[23:16]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.340 IMEM_SRAM_APEX_REG_2251

Name: IMEM_SRAM_APEX_REG_2251
Address: 2251 (8CBh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[31:24]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.341 IMEM_SRAM_APEX_REG_2252

Name: IMEM_SRAM_APEX_REG_2252
Address: 2252 (8CCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[39:32]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.342 IMEM_SRAM_APEX_REG_2253

Name: IMEM_SRAM_APEX_REG_2253
Address: 2253 (8CDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[47:40]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.343 IMEM_SRAM_APEX_REG_2254

Name: IMEM_SRAM_APEX_REG_2254
Address: 2254 (8CEh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[55:48]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.344 IMEM_SRAM_APEX_REG_2255

Name: IMEM_SRAM_APEX_REG_2255
Address: 2255 (8CFh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[63:56]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.345 IMEM_SRAM_APEX_REG_2256

Name: IMEM_SRAM_APEX_REG_2256
Address: 2256 (8D0h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[71:64]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.346 IMEM_SRAM_APEX_REG_2257

Name: IMEM_SRAM_APEX_REG_2257
Address: 2257 (8D1h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[79:72]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.347 IMEM_SRAM_APEX_REG_2258

Name: IMEM_SRAM_APEX_REG_2258
Address: 2258 (8D2h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[87:80]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.348 IMEM_SRAM_APEX_REG_2259

Name: IMEM_SRAM_APEX_REG_2259
Address: 2259 (8D3h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_BIAS_1G_Q16[95:88]	Accelerometer bias to start with (one value per axis). Unit: g in s32q16 Default: 0;0;0

18.349 IMEM_SRAM_APEX_REG_2339

Name: IMEM_SRAM_APEX_REG_2339
Address: 2339 (923h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_SAVED_ACC_ACCURACY[7:0]	Accelerometer accuracy from 0 (non-calibrated) to 3 (well-calibrated). Range: [0 - 3] Default: 0

18.350 IMEM_SRAM_APEX_REG_2340

Name: IMEM_SRAM_APEX_REG_2340
Address: 2340 (924h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_INIT_STATUS[7:0]	GAF initialization status. Set to 1 by eDMP once GAF initialization is done. Default: 0 (GAF initialization not performed)

18.351 IMEM_SRAM_APEX_REG_2412

Name: IMEM_SRAM_APEX_REG_2412
Address: 2412 (96Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[7:0]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.352 IMEM_SRAM_APEX_REG_2413

Name: IMEM_SRAM_APEX_REG_2413
Address: 2413 (96Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[15:8]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.353 IMEM_SRAM_APEX_REG_2414

Name: IMEM_SRAM_APEX_REG_2414
Address: 2414 (96Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[23:16]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.354 IMEM_SRAM_APEX_REG_2415

Name: IMEM_SRAM_APEX_REG_2415
Address: 2415 (96Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[31:24]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.355 IMEM_SRAM_APEX_REG_2416

Name: IMEM_SRAM_APEX_REG_2416
Address: 2416 (970h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[39:32]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.356 IMEM_SRAM_APEX_REG_2417

Name: IMEM_SRAM_APEX_REG_2417
Address: 2417 (971h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_GYR_BIAS_DPS_Q12[47:40]	Latest gyroscope bias computed to be saved (one value per axis). Unit: dps in s32q12 Default: 0;0;0

18.357 IMEM_SRAM_APEX_REG_2420

Name: IMEM_SRAM_APEX_REG_2420
Address: 2420 (974h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[7:0]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.358 IMEM_SRAM_APEX_REG_2421

Name: IMEM_SRAM_APEX_REG_2421
Address: 2421 (975h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[15:8]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.359 IMEM_SRAM_APEX_REG_2422

Name: IMEM_SRAM_APEX_REG_2422
Address: 2422 (976h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[23:16]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.360 IMEM_SRAM_APEX_REG_2423

Name: IMEM_SRAM_APEX_REG_2423
Address: 2423 (977h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[31:24]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.361 IMEM_SRAM_APEX_REG_2424

Name: IMEM_SRAM_APEX_REG_2424
Address: 2424 (978h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[39:32]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.362 IMEM_SRAM_APEX_REG_2425

Name: IMEM_SRAM_APEX_REG_2425
Address: 2425 (979h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[47:40]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.363 IMEM_SRAM_APEX_REG_2426

Name: IMEM_SRAM_APEX_REG_2426
Address: 2426 (97Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[55:48]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.364 IMEM_SRAM_APEX_REG_2427

Name: IMEM_SRAM_APEX_REG_2427
Address: 2427 (97Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[63:56]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.365 IMEM_SRAM_APEX_REG_2428

Name: IMEM_SRAM_APEX_REG_2428
Address: 2428 (97Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[71:64]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.366 IMEM_SRAM_APEX_REG_2429

Name: IMEM_SRAM_APEX_REG_2429
Address: 2429 (97Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[79:72]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.367 IMEM_SRAM_APEX_REG_2430

Name: IMEM_SRAM_APEX_REG_2430
Address: 2430 (97Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[87:80]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.368 IMEM_SRAM_APEX_REG_2431

Name: IMEM_SRAM_APEX_REG_2431
Address: 2431 (97Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_BIAS_UT_Q16[95:88]	Latest magnetometer bias computed to be saved (one value per axis), any new mag bias must also be applied in this RAM area. Unit: µT in s32q16 Default: 0;0;0

18.369 IMEM_SRAM_APEX_REG_2433

Name: IMEM_SRAM_APEX_REG_2433
Address: 2433 (981h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GAF_READ_MAG_ACCURACY[7:0]	Latest magnetometer accuracy from 0 (non calibrated) to 3 (well calibrated) to be saved. Range: [0 - 3] Default: 0

18.370 IMEM_SRAM_APEX_REG_2524

Name: IMEM_SRAM_APEX_REG_2524
Address: 2524 (9DCh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TIME_FEAS_CONFIG[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.371 IMEM_SRAM_APEX_REG_2525

Name: IMEM_SRAM_APEX_REG_2525
Address: 2525 (9DDh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TIME_FEAS_CONFIG[15:8]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.372 IMEM_SRAM_APEX_REG_2548

Name: IMEM_SRAM_APEX_REG_2548
Address: 2548 (9F4h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CLASS_INDEX[7:0]	Index of SIF predicted gesture class.

18.373 IMEM_SRAM_APEX_REG_2549

Name: IMEM_SRAM_APEX_REG_2549
Address: 2549 (9F5h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CLASS_INDEX[15:8]	Index of SIF predicted gesture class.

18.374 IMEM_SRAM_APEX_REG_2612

Name: IMEM_SRAM_APEX_REG_2612
Address: 2612 (A34h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.375 IMEM_SRAM_APEX_REG_2613

Name: IMEM_SRAM_APEX_REG_2613
Address: 2613 (A35h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[15:8]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.376 IMEM_SRAM_APEX_REG_2614

Name: IMEM_SRAM_APEX_REG_2614
Address: 2614 (A36h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[23:16]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.377 IMEM_SRAM_APEX_REG_2615

Name: IMEM_SRAM_APEX_REG_2615
Address: 2615 (A37h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[31:24]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.378 IMEM_SRAM_APEX_REG_2616

Name: IMEM_SRAM_APEX_REG_2616
Address: 2616 (A38h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[39:32]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.379 IMEM_SRAM_APEX_REG_2617

Name: IMEM_SRAM_APEX_REG_2617
Address: 2617 (A39h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[47:40]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.380 IMEM_SRAM_APEX_REG_2618

Name: IMEM_SRAM_APEX_REG_2618
Address: 2618 (A3Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[55:48]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.381 IMEM_SRAM_APEX_REG_2619

Name: IMEM_SRAM_APEX_REG_2619
Address: 2619 (A3Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[63:56]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.382 IMEM_SRAM_APEX_REG_2620

Name: IMEM_SRAM_APEX_REG_2620
Address: 2620 (A3Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[71:64]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.383 IMEM_SRAM_APEX_REG_2621

Name: IMEM_SRAM_APEX_REG_2621
Address: 2621 (A3Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[79:72]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.384 IMEM_SRAM_APEX_REG_2622

Name: IMEM_SRAM_APEX_REG_2622
Address: 2622 (A3Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[87:80]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.385 IMEM_SRAM_APEX_REG_2623

Name: IMEM_SRAM_APEX_REG_2623
Address: 2623 (A3Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_CCONFIG[95:88]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.386 IMEM_SRAM_APEX_REG_2624

Name: IMEM_SRAM_APEX_REG_2624
Address: 2624 (A40h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.387 IMEM_SRAM_APEX_REG_2625

Name: IMEM_SRAM_APEX_REG_2625
Address: 2625 (A41h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[15:8]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.388 IMEM_SRAM_APEX_REG_2626

Name: IMEM_SRAM_APEX_REG_2626
Address: 2626 (A42h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[23:16]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.389 IMEM_SRAM_APEX_REG_2627

Name: IMEM_SRAM_APEX_REG_2627
Address: 2627 (A43h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[31:24]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.390 IMEM_SRAM_APEX_REG_2628

Name: IMEM_SRAM_APEX_REG_2628
Address: 2628 (A44h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[39:32]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.391 IMEM_SRAM_APEX_REG_2629

Name: IMEM_SRAM_APEX_REG_2629
Address: 2629 (A45h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[47:40]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.392 IMEM_SRAM_APEX_REG_2630

Name: IMEM_SRAM_APEX_REG_2630
Address: 2630 (A46h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[55:48]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.393 IMEM_SRAM_APEX_REG_2631

Name: IMEM_SRAM_APEX_REG_2631
Address: 2631 (A47h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[63:56]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.394 IMEM_SRAM_APEX_REG_2632

Name: IMEM_SRAM_APEX_REG_2632
Address: 2632 (A48h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[71:64]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.395 IMEM_SRAM_APEX_REG_2633

Name: IMEM_SRAM_APEX_REG_2633
Address: 2633 (A49h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[79:72]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.396 IMEM_SRAM_APEX_REG_2634

Name: IMEM_SRAM_APEX_REG_2634
Address: 2634 (A4Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[87:80]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.397 IMEM_SRAM_APEX_REG_2635

Name: IMEM_SRAM_APEX_REG_2635
Address: 2635 (A4Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[95:88]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.398 IMEM_SRAM_APEX_REG_2636

Name: IMEM_SRAM_APEX_REG_2636
Address: 2636 (A4Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[103:96]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.399 IMEM_SRAM_APEX_REG_2637

Name: IMEM_SRAM_APEX_REG_2637
Address: 2637 (A4Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[111:104]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.400 IMEM_SRAM_APEX_REG_2638

Name: IMEM_SRAM_APEX_REG_2638
Address: 2638 (A4Eh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[119:112]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.401 IMEM_SRAM_APEX_REG_2639

Name: IMEM_SRAM_APEX_REG_2639
Address: 2639 (A4Fh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[127:120]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.402 IMEM_SRAM_APEX_REG_2640

Name: IMEM_SRAM_APEX_REG_2640
Address: 2640 (A50h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[135:128]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.403 IMEM_SRAM_APEX_REG_2641

Name: IMEM_SRAM_APEX_REG_2641
Address: 2641 (A51h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[143:136]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.404 IMEM_SRAM_APEX_REG_2642

Name: IMEM_SRAM_APEX_REG_2642
Address: 2642 (A52h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[151:144]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.405 IMEM_SRAM_APEX_REG_2643

Name: IMEM_SRAM_APEX_REG_2643
Address: 2643 (A53h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[159:152]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.406 IMEM_SRAM_APEX_REG_2644

Name: IMEM_SRAM_APEX_REG_2644
Address: 2644 (A54h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[167:160]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.407 IMEM_SRAM_APEX_REG_2645

Name: IMEM_SRAM_APEX_REG_2645
Address: 2645 (A55h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[175:168]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.408 IMEM_SRAM_APEX_REG_2646

Name: IMEM_SRAM_APEX_REG_2646
Address: 2646 (A56h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[183:176]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.409 IMEM_SRAM_APEX_REG_2647

Name: IMEM_SRAM_APEX_REG_2647
Address: 2647 (A57h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TCONFIG[191:184]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.410 IMEM_SRAM_APEX_REG_2652 TO IMEM_SRAM_APEX_REG_2727

Name: IMEM_SRAM_APEX_REG_2652 to IMEM_SRAM_APEX_REG_2727
Address: 2652 to 2727 (A5Ch to AA7h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_FILTER[607:0]	SIF Filter state structure with filter coefficients and buffer. Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.411 IMEM_SRAM_APEX_REG_5004

Name: IMEM_SRAM_APEX_REG_5004
Address: 5004 (138Ch)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TREE_THRESHOLDS[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.412 IMEM_SRAM_APEX_REG_5005

Name: IMEM_SRAM_APEX_REG_5005
Address: 5005 (138Dh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TREE_THRESHOLDS[15:8]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.413 IMEM_SRAM_APEX_REG_5514

Name: IMEM_SRAM_APEX_REG_5514
Address: 5514 (158Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TREE_FEATUREIDS[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.414 IMEM_SRAM_APEX_REG_5769

Name: IMEM_SRAM_APEX_REG_5769
Address: 5769 (1689h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TREE_NEXTNODERIGHT[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

18.415 IMEM_SRAM_APEX_REG_6024

Name: IMEM_SRAM_APEX_REG_6024
Address: 6024 (1788h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SIF_TREE_THRESHOLDSSHIFT[7:0]	Structure member of the SIF model Decision Tree generated with TDK SIF software tools. Must be loaded as-is based on TDK recommendation.

19 USER BANK IMEM_SRAM_STC REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IMEM_SRAM_STC. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

19.1 IMEM_SRAM_STC_REG_52

Name: IMEM_SRAM_STC_REG_52
Address: 52 (34h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_CONFIGPARAMS[7:0]	Self-test input parameters bit0: If set, enable self-test init, must be set when any of accel or gyro self-test enable bit is set (bits 2:1) bit1: If set, enable accel self-test bit2: If set, enable gyro self-test bit3~6: Unused bit7~9: Averaging time used to perform self-test (0/1/2/3/4/5: 10/20/40/80/160/320 ms) bit10~12: Tolerance between factory trim and accel self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%) bit13~15: Tolerance between factory trim and gyro self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%)

19.2 IMEM_SRAM_STC_REG_53

Name: IMEM_SRAM_STC_REG_53
Address: 53 (35h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_CONFIGPARAMS[15:8]	Self-test input parameters bit0: If set, enable self-test init, must be set when any of accel or gyro self-test enable bit is set (bits 2:1) bit1: If set, enable accel self-test bit2: If set, enable gyro self-test bit3~6: Unused bit7~9: Averaging time used to perform self-test (0/1/2/3/4/5: 10/20/40/80/160/320 ms) bit10~12: Tolerance between factory trim and accel self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%) bit13~15: Tolerance between factory trim and gyro self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%)

19.3 IMEM_SRAM_STC_REG_54

Name: IMEM_SRAM_STC_REG_54
Address: 54 (36h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_CONFIGPARAMS[23:16]	Self-test input parameters bit0: If set, enable self-test init, must be set when any of accel or gyro self-test enable bit is set (bits 2:1) bit1: If set, enable accel self-test bit2: If set, enable gyro self-test bit3~6: Unused bit7~9: Averaging time used to perform self-test (0/1/2/3/4/5: 10/20/40/80/160/320 ms) bit10~12: Tolerance between factory trim and accel self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%) bit13~15: Tolerance between factory trim and gyro self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%)

19.4 IMEM_SRAM_STC_REG_55

Name: IMEM_SRAM_STC_REG_55
Address: 55 (37h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_CONFIGPARAMS[31:24]	Self-test input parameters bit0: If set, enable self-test init, must be set when any of accel or gyro self-test enable bit is set (bits 2:1) bit1: If set, enable accel self-test bit2: If set, enable gyro self-test bit3~6: Unused bit7~9: Averaging time used to perform self-test (0/1/2/3/4/5: 10/20/40/80/160/320 ms) bit10~12: Tolerance between factory trim and accel self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%) bit13~15: Tolerance between factory trim and gyro self-test response (0/1/2/3/4/5/6/7: 5/10/15/20/25/30/40/50%)

19.5 IMEM_SRAM_STC_REG_56

Name: IMEM_SRAM_STC_REG_56
Address: 56 (38h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_RESULTS[7:0]	Results/status from self-test run bit0: AX Self-test result (0:pass 1:fail) bit1: AY Self-test result (0:pass 1:fail) bit2: AZ Self-test result (0:pass 1:fail) bit3: GX Self-test result (0:pass 1:fail) bit4: GY Self-test result (0:pass 1:fail) bit5: GZ Self-test result (0:pass 1:fail) bit6~7: Self-test status (0:Done 1:InProgress)

19.6 IMEM_SRAM_STC_REG_57

Name: IMEM_SRAM_STC_REG_57
Address: 57 (39h)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_RESULTS[15:8]	Results/status from self-test run bit0: AX Self-test result (0:pass 1:fail) bit1: AY Self-test result (0:pass 1:fail) bit2: AZ Self-test result (0:pass 1:fail) bit3: GX Self-test result (0:pass 1:fail) bit4: GY Self-test result (0:pass 1:fail) bit5: GZ Self-test result (0:pass 1:fail) bit6~7: Self-test status (0:Done 1:InProgress)

19.7 IMEM_SRAM_STC_REG_58

Name: IMEM_SRAM_STC_REG_58
Address: 58 (3Ah)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_RESULTS[23:16]	Results/status from self-test run bit0: AX Self-test result (0:pass 1:fail) bit1: AY Self-test result (0:pass 1:fail) bit2: AZ Self-test result (0:pass 1:fail) bit3: GX Self-test result (0:pass 1:fail) bit4: GY Self-test result (0:pass 1:fail) bit5: GZ Self-test result (0:pass 1:fail) bit6~7: Self-test status (0:Done 1:InProgress)

19.8 IMEM_SRAM_STC_REG_59

Name: IMEM_SRAM_STC_REG_59
Address: 59 (3Bh)
Serial IF: R/W
Reset value: Random value after reset until host runs EDMP_INIT procedure
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	STC_RESULTS[31:24]	Results/status from self-test run bit0: AX Self-test result (0:pass 1:fail) bit1: AY Self-test result (0:pass 1:fail) bit2: AZ Self-test result (0:pass 1:fail) bit3: GX Self-test result (0:pass 1:fail) bit4: GY Self-test result (0:pass 1:fail) bit5: GZ Self-test result (0:pass 1:fail) bit6~7: Self-test status (0:Done 1:InProgress)

20 USER BANK IPREG_BAR REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_BAR. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

20.1 IPREG_BAR_REG_57

Name: IPREG_BAR_REG_57
Address: 57 (39h)
Serial IF: R/W
Reset value: 0x32
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	IO_OPT0	Set this register field to 1 for optimal speed of IOs. IO_OPT1 must be also set to 1 if IO_OPT0 is set to 1. Can be changed on-the-fly.
5	IO_OPT1	Set this register field to 1 for optimal speed of IOs. Can be changed on-the-fly.
4:0	-	Reserved

20.2 IPREG_BAR_REG_58

Name: IPREG_BAR_REG_58
Address: 58 (3Ah)
Serial IF: R/W
Reset value: 0xD9
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	PADS_AP_SCLK_PUD_TRIM_D2A	Selects internal resistor pull direction for AP_SCLK pin (pin 13) 0: Down 1: Up Can be changed on-the-fly.
6	PADS_AP_SCLK_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AP_SCLK pin (pin 13), depending on direction selected by bit 7. 0: Not enabled 1: Enabled Can be changed on-the-fly.
5	-	Reserved
4	PADS_AP_CS_PUD_TRIM_D2A	Selects internal resistor pull direction for AP_CS pin (pin 12) 0: Down 1: Up Can be changed on-the-fly.
3	PADS_AP_CS_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AP_CS pin (pin 12), depending on direction selected by bit 4. 0: Not enabled 1: Enabled Can be changed on-the-fly.
2:1	-	Reserved
0	IO_OPT2	Set this register field to 1 for optimal speed of IOs. IO_OPT1 must be also set to 1 if IO_OPT2 is set to 1 Can be changed on-the-fly.

20.3 IPREG_BAR_REG_59

Name: IPREG_BAR_REG_59
Address: 59 (3Bh)
Serial IF: R/W
Reset value: 0x96
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	PADS_PIN7_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for pin 7, depending on direction selected by bit 0 of register IPREG_BAR_REG_60 0: Not enabled 1: Enabled Can be changed on-the-fly.
6	-	Reserved
5	PADS_AP_SDO_PUD_TRIM_D2A	Selects internal resistor pull direction for AP_SDO pin (pin 1) 0: Down 1: Up Can be changed on-the-fly.
4	PADS_AP_SDO_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AP_SDO pin (pin 1), depending on direction selected by bit 5. 0: Not enabled 1: Enabled Can be changed on-the-fly.
3	-	Reserved
2	PADS_AP_SDI_PUD_TRIM_D2A	Selects internal resistor pull direction for AP_SDI pin (pin 14) 0: Down 1: Up Can be changed on-the-fly.
1	PADS_AP_SDI_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AP_SDI pin (pin 14), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly.
0	-	Reserved

20.4 IPREG_BAR_REG_60

Name: IPREG_BAR_REG_60
Address: 60 (3Ch)
Serial IF: R/W
Reset value: 0x7D
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	PADS_AUX1_SCLK_PUD_TRIM_D2A	Selects internal resistor pull direction for AUX1_SCLK pin (pin 3) 0: Down 1: Up Can be changed on-the-fly.
5	PADS_AUX1_SCLK_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AUX1_SCLK pin (pin 3), depending on direction selected by bit 6. 0: Not enabled 1: Enabled Can be changed on-the-fly.
4	PADS_AUX_SCLK_TP2_FROM_PAD_DISABLE_TRIM_D2A	Set this bit to 1 if using I^2C master mode. Set it to 0 otherwise.
3	PADS_AUX1_CS_PUD_TRIM_D2A	Selects internal resistor pull direction for AUX1_CS pin (pin 10) 0: Down 1: Up Can be changed on-the-fly.
2	PADS_AUX1_CS_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AUX1_CS pin (pin 10), depending on direction selected by bit 3. 0: Not enabled 1: Enabled Can be changed on-the-fly.
1	-	Reserved
0	PADS_PIN7_CS_PUD_TRIM_D2A	Selects internal resistor pull direction for pin 7 0: Down 1: Up Can be changed on-the-fly.

20.5 IPREG_BAR_REG_61

Name: IPREG_BAR_REG_61
Address: 61 (3Dh)
Serial IF: R/W
Reset value: 0xBB
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	PADS_INT1_PUD_TRIM_D2A	Selects internal resistor pull direction for INT1 pin (pin 4) 0: Down 1: Up Can be changed on-the-fly.
6	PADS_INT1_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for INT1 pin (pin 4), depending on direction selected by bit 7. 0: Not enabled 1: Enabled Can be changed on-the-fly.
5	-	Reserved
4	PADS_AUX1_SDO_PUD_TRIM_D2A	Selects internal resistor pull direction for AUX1_SDO pin (pin 11) 0: Down 1: Up Can be changed on-the-fly.
3	PADS_AUX1_SDO_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AUX1_SDO pin (pin 11), depending on direction selected by bit 4. 0: Not enabled 1: Enabled Can be changed on-the-fly.
2	-	Reserved
1	PADS_AUX1_SDI_PUD_TRIM_D2A	Selects internal resistor pull direction for AUX1_SDI pin (pin 2) 0: Down 1: Up Can be changed on-the-fly.
0	PADS_AUX1_SDI_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for AUX1_SDI pin (pin 2), depending on direction selected by bit 1. 0: Not enabled 1: Enabled Can be changed on-the-fly.

20.6 IPREG_BAR_REG_62

Name: IPREG_BAR_REG_62
Address: 62 (3Eh)
Serial IF: R/W
Reset value: 0x06
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2	PADS_INT2_PUD_TRIM_D2A	Selects internal resistor pull direction for INT2 pin (pin 9) 0: Down 1: Up Can be changed on-the-fly.
1	PADS_INT2_PE_TRIM_D2A	Enables internal pull resistor to pull up or down for INT2 pin (pin 9), depending on direction selected by bit 2. 0: Not enabled 1: Enabled Can be changed on-the-fly.
0	-	Reserved

21 USER BANK IPREG_TOP1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_TOP1. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

21.1 I2CM_COMMAND_0

Name: I2CM_COMMAND_0 (I^2C master command buffer 0)
Address: 06 (06h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	ENDFLAG_0	Indicates if the current entry is the last I^2C master communication with the external slave device.
6	CH_SEL_0	Specifies the channel number for I^2C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID “ID1” 1: Specify the other external sensor with device ID “ID2” “ID1” and “ID2” should be replaced by the actual device ID of the chosen external devices.
5:4	R_W_0	I^2C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved
3:0	BURSTLEN_0	Specifies the burst length of I^2C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111.

21.2 I2CM_COMMAND_1

Name: I2CM_COMMAND_1 (I^2C master command buffer 1)
Address: 07 (07h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	ENDFLAG_1	Indicates if the current entry is the last I^2C master communication with the external slave device.
6	CH_SEL_1	Specifies the channel number for I^2C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID “ID1” 1: Specify the other external sensor with device ID “ID2” “ID1” and “ID2” should be replaced by the actual device ID of the chosen external devices.
5:4	R_W_1	I^2C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved
3:0	BURSTLEN_1	Specifies the burst length of I^2C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111.

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21.3 I2CM_COMMAND_2

Name: I2CM_COMMAND_2 (I^2C master command buffer 2)
Address: 08 (08h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	ENDFLAG_2	Indicates if the current entry is the last I^2C master communication with the external slave device.
6	CH_SEL_2	Specifies the channel number for I^2C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID “ID1” 1: Specify the other external sensor with device ID “ID2” “ID1” and “ID2” should be replaced by the actual device ID of the chosen external devices.
5:4	R_W_2	I^2C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved
3:0	BURSTLEN_2	Specifies the burst length of I^2C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111.

21.4 I2CM_COMMAND_3

Name: I2CM_COMMAND_3 (I^2C master command buffer 3)
Address: 09 (09h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	ENDFLAG_3	Indicates if the current entry is the last I^2C master communication with the external slave device.
6	CH_SEL_3	Specifies the channel number for I^2C master transaction. Two external sensors are supported. 0: Specify one external sensor with device ID “ID1” 1: Specify the other external sensor with device ID “ID2” “ID1” and “ID2” should be replaced by the actual device ID of the chosen external devices.
5:4	R_W_3	I^2C master read/write command. 00: Write operation 01: Read operation with register address specified 10: Read operation without register address specified 11: Reserved
3:0	BURSTLEN_3	Specifies the burst length of I^2C master communication with the external slave device. 0000: Reserved 0001: 1 byte 0010: 2 bytes 0011: 3 bytes 0100: 4 bytes 0101: 5 bytes 0110: 6 bytes 0111: 7 bytes 1000: 8 bytes 1001: 9 bytes 1010: 10 bytes 1011: 11 bytes 1100: 12 bytes 1101: 13 bytes 1110: 14 bytes 1111: 15 bytes Note: For write operation the valid values are 0001 to 0110; For read operation the valid values are 0001 to 1111.

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21.5 I2CM_DEV_PROFILE0

Name: I2CM_DEV_PROFILE0
Address: 14 (0Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	RD_ADDRESS_0	Specifies the read address for channel 0 I^2C master transaction

21.6 I2CM_DEV_PROFILE1

Name: I2CM_DEV_PROFILE1
Address: 15 (0Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6:0	DEV_ID_0	Specifies the slave ID for channel 0 I^2C master transaction

21.7 I2CM_DEV_PROFILE2

Name: I2CM_DEV_PROFILE2
Address: 16 (10h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	RD_ADDRESS_1	Specifies the read address for channel 1 I^2C master transaction

21.8 I2CM_DEV_PROFILE3

Name: I2CM_DEV_PROFILE3
Address: 17 (11h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6:0	DEV_ID_1	Specifies the slave ID for channel 1 I^2C master transaction

21.9 I2CM_CONTROL

Name: I2CM_CONTROL
Address: 22 (16h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6	I2CM_RESTART_EN	0: No Restart is used 1: In an I2C register read transaction, the Restart is used to bridge the register-address write transaction and register-data read transaction. This bit is not programmable by MCU when I2CM_BUSY = 1.
5:4	-	Reserved
3	I2CM_SPEED	0: I^2C Fast Mode 1: I^2C Standard Mode
2:1	-	Reserved
0	I2CM_GO	1: Kicks off I^2C master operation. Clears to 0 after I^2C master operation is completed. This bit is not programmable when I2CM_BUSY = 1

21.10 I2CM_STATUS

Name: I2CM_STATUS
Address: 24 (18h)
Serial IF: R
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	I2CM_SDA_ERR	I2C master SDA error indication
4	I2CM_SCL_ERR	I2C master SCL error indication
3	I2CM_SRST_ERR	I2C master SRST error indication
2	I2CM_TIMEOUT_ERR	I2C master timeout error indication
1	I2CM_DONE	1: Status bit, indicates I^2C master operation has completed, with or without errors. This bit is cleared due to (a) MCU read or (b) when I2CM_GO is programmed to 1 or (c) ODR event for fetching sensor data from the external sensor.
0	I2CM_BUSY	0: Indicates no I^2C master operation is running 1: Indicates I^2C master operation is running

21.11 I2CM_EXT_DEV_STATUS

Name: I2CM_EXT_DEV_STATUS
Address: 26 (1Ah)
Serial IF: R/C
Reset value: 0x0F
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	I2CM_EXT_DEV_STATUS	Indicates ACK/NACK feedback from the external device per each entry of the command buffer. I2CM_EXT_DEV_STATUS is set to 0xF whenever I^2C master operation is kicked off. Bit 0 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_0. 0: ACK 1: NACK Bit 1 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_1. 0: ACK 1: NACK Bit 2 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_2. 0: ACK 1: NACK Bit 3 of I2CM_EXT_DEV_STATUS: ACK/NACK feedback from the external device to I2CM_COMMAND_3. 0: ACK 1: NACK

21.12 I2CM_RD_DATA0

Name: I2CM_RD_DATA0
Address: 27 (1Bh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA0	The 1st byte received from I^2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.13 I2CM_RD_DATA1

Name: I2CM_RD_DATA1
Address: 28 (1Ch)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA1	The 2nd byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.14 I2CM_RD_DATA2

Name: I2CM_RD_DATA2
Address: 29 (1Dh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA2	The 3rd byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.15 I2CM_RD_DATA3

Name: I2CM_RD_DATA3
Address: 30 (1Eh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA3	The 4th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.16 I2CM_RD_DATA4

Name: I2CM_RD_DATA4
Address: 31 (1Fh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA4	The 5th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.17 I2CM_RD_DATA5

Name: I2CM_RD_DATA5
Address: 32 (20h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA5	The 6th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.18 I2CM_RD_DATA6

Name: I2CM_RD_DATA6
Address: 33 (21h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA6	The 7th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.19 I2CM_RD_DATA7

Name: I2CM_RD_DATA7
Address: 34 (22h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA7	The 8th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.20 I2CM_RD_DATA8

Name: I2CM_RD_DATA8
Address: 35 (23h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA8	The 9th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.21 I2CM_RD_DATA9

Name: I2CM_RD_DATA9
Address: 36 (24h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA9	The 10th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.22 I2CM_RD_DATA10

Name: I2CM_RD_DATA10
Address: 37 (25h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA10	The 11th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.23 I2CM_RD_DATA11

Name: I2CM_RD_DATA11
Address: 38 (26h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA11	The 12th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.24 I2CM_RD_DATA12

Name: I2CM_RD_DATA12
Address: 39 (27h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA12	The 13th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.25 I2CM_RD_DATA13

Name: I2CM_RD_DATA13
Address: 40 (28h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA13	The 14th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.26 I2CM_RD_DATA14

Name: I2CM_RD_DATA14
Address: 41 (29h)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA14	The 15th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.27 I2CM_RD_DATA15

Name: I2CM_RD_DATA15
Address: 42 (2Ah)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA15	The 16th byte received from I²C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.28 I2CM_RD_DATA16

Name: I2CM_RD_DATA16
Address: 43 (2Bh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA16	The 17th byte received from I²C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.29 I2CM_RD_DATA17

Name: I2CM_RD_DATA17
Address: 44 (2Ch)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA17	The 18th byte received from I²C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.30 I2CM_RD_DATA18

Name: I2CM_RD_DATA18
Address: 45 (2Dh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA18	The 19th byte received from I²C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.31 I2CM_RD_DATA19

Name: I2CM_RD_DATA19
Address: 46 (2Eh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA19	The 20th byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.32 I2CM_RD_STATUS20

Name: I2CM_RD_DATA20
Address: 47 (2Fh)
Serial IF: RWS
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_RD_DATA20	The 21st byte received from I2C slave. Content of this register is automatically cleared to 0 when I2CM_GO = 1 or upon ODR event for fetching sensor data from the external sensor.

21.33 I2CM_WR_DATA0

Name: I2CM_WR_DATA0
Address: 51 (33h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA0	The data/address byte for a Write transaction.

21.34 I2CM_WR_DATA1

Name: I2CM_WR_DATA1
Address: 52 (34h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA1	The data/address byte for a Write transaction.

21.35 I2CM_WR_DATA2

Name: I2CM_WR_DATA2
Address: 53 (35h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA2	The data/address byte for a Write transaction.

21.36 I2CM_WR_DATA3

Name: I2CM_WR_DATA3
Address: 54 (36h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA3	The data/address byte for a Write transaction.

21.37 I2CM_WR_DATA4

Name: I2CM_WR_DATA4
Address: 55 (37h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA4	The data/address byte for a Write transaction.

21.38 I2CM_WR_DATA5

Name: I2CM_WR_DATA5
Address: 56 (38h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	I2CM_WR_DATA5	The data/address byte for a Write transaction.

21.39 SIFS_IXC_ERROR_STATUS

Name: SIFS_IXC_ERROR_STATUS
Address: 75 (4Bh)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	AUX1_SIFS_IXC_TIMEOUT_ERR	0: No timeout error. 1: Indicates than an IxC timeout error occurred in AUX1 SIFS. No clock toggle condition from host for 32ms while an IxC transaction was ongoing (after START and before STOP).
0	SIFS_IXC_TIMEOUT_ERR	0: No timeout error or when SPI slave is selected for serial transfers. 1: Indicates than an IxC timeout error occurred in SIFS. No clock toggle condition from host for 32ms while an IxC transaction was ongoing (after START and before STOP).

21.40 EDMP_PRGRM_IRQ0_0

Name: EDMP_PRGRM_IRQ0_0
Address: 79 (4Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_0[7:0]	Start address of IRQ_0 vector. Can be changed on-the-fly.

21.41 EDMP_PRGRM_IRQ0_1

Name: EDMP_PRGRM_IRQ0_1
Address: 80 (50h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_0[15:8]	Start address of IRQ_0 vector. Can be changed on-the-fly.

21.42 EDMP_PRGRM_IRQ1_0

Name: EDMP_PRGRM_IRQ1_0
Address: 81 (51h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_1[7:0]	Start address of IRQ_1 vector. Can be changed on-the-fly.

21.43 EDMP_PRGRM_IRQ1_1

Name: EDMP_PRGRM_IRQ1_1
Address: 82 (52h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_1[15:8]	Start address of IRQ_1 vector. Can be changed on-the-fly.

21.44 EDMP_PRGRM_IRQ2_0

Name: EDMP_PRGRM_IRQ2_0
Address: 83 (53h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_2[7:0]	Start address of IRQ_2 vector. Can be changed on-the-fly.

21.45 EDMP_PRGRM_IRQ2_1

Name: EDMP_PRGRM_IRQ2_1
Address: 84 (54h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	PRGRM_STRT_ADDR_IRQ_2[15:8]	Start address of IRQ_2 vector. Can be changed on-the-fly.

21.46 EDMP_SP_START_ADDR

Name: EDMP_SP_START_ADDR
Address: 85 (55h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	EDMP_SP_START_ADDR	Sets eDMP stack address. Can be changed on-the-fly.

21.47 SMC_CONTROL_0

Name: SMC_CONTROL_0
Address: 88 (58h)
Serial IF: R/W
Reset value: 0x60
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:5	-	Reserved
4	ACCEL_LP_CLK_SEL	This bit is applicable to host interface operation. A. When RTC mode is not enabled (or RTC_MODE = 0): This bit is effective when the host interface is in accel only operation with ACCEL_MODE set to LP mode. 0: Host interface is in AULP mode. 1: Host interface is in ALP mode. When I3C^{SM} Synchronous Timing Control function is enabled on host interface, if the host interface is in accel only operation with ACCEL_MODE set to LP mode, ACCEL_LP_CLK_SEL must be set to 1. I3C^{SM} Synchronous Timing Control may not generate correct timing if ACCEL_LP_CLK_SEL is set to 0. B. When RTC mode is enabled (or RTC_MODE = 1): Independent of enabling/disabling of I3C^{SM} Synchronous timing control function, ACCEL_LP_CLK_SEL must be set to 1. Dynamic Change Supported.
3	TEMP_DIS	0: Temperature Sensor not disabled. 1: Temperature Sensor disabled.
2	TMST_FORCE_AUX_FINE_EN	0: Time Stamp fine counting enabled only on UI interface. 1: Time Stamp fine counting enabled on AUX interfaces in addition to UI interface.
1	TMST_FSYNC_EN	Time Stamp register FSYNC Enable. 0: Timestamp feature of FSYNC not enabled. 1: Timestamp feature of FSYNC enabled.
0	TMST_EN	0: Timestamp not enabled.

		1: Timestamp enabled.

21.48 SMC_CONTROL_1

Name: SMC_CONTROL_1
Address: 89 (59h)
Serial IF: R/W
Reset value: 0x04
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3	SREG_AUX_ACCEL_ONLY_EN	0: Sensor data register read from AUX1 interface is supported only if gyro sensor is enabled. 1: Sensor data register read from AUX1 interface is supported even if gyro sensor is not enabled.
2:0	-	Reserved

21.49 STC_CONFIG

Name: STC_CONFIG
Address: 99 (63h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:2	STC_SENSOR_SEL	Sensor that controls STC: 0 or 1: Slowest ODR sensor 2: Accel 3: Gyro
1:0	-	Reserved

21.50 SREG_CTRL

Name: SREG_CTRL
Address: 103 (67h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	SREG_DATA_ENDIAN_SEL	Selects Endianness of Sensor Data Registers and FIFO data 0: Sensor data, FIFO data, and FIFO count is in Little Endian format 1: Sensor data, FIFO data, and FIFO count is in Big Endian format Note: User must set register field SREG_DATA_ENDIAN_SEL to 1, to enable Big Endian data format for data in Sensor Data Registers and FIFO, and for FIFO Count.
0	-	Reserved

21.51 SIFS_I3C_STC_CFG

Name: SIFS_I3C_STC_CFG
Address: 104 (68h)
Serial IF: R/W
Reset value: 0x23
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2	I3C_STC_MODE	Enable the STC controller 0: Disable I3C STC. 1: Enable I3C STC. Toggling this bit restarts the ODR frequency and phase correction operation as if the chip is out of reset. The STC functionality can be enabled only if ACCEL_LP_CLK_SEL is set to 1; otherwise device may not behave as expected.
1:0	-	Reserved

21.52 INT_PULSE_MIN_ON_INTF0

Name: INT_PULSE_MIN_ON_INTF0
Address: 105 (69h)
Serial IF: R/W
Reset value: 0x01
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	INT0_TPULSE_DURATION	INT0 interrupt pulse minimum “on” duration for host interface, when in pulse mode. 0: 100µs (use only if ODR < 4kHz) 1: 8µs (required if ODR ≥ 4kHz, optional for ODR < 4kHz) Other Settings: Reserved

21.53 INT_PULSE_MIN_ON_INTF1

Name: INT_PULSE_MIN_ON_INTF1
Address: 106 (6Ah)
Serial IF: R/W
Reset value: 0x01
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	INT1_TPULSE_DURATION	INT1 interrupt pulse minimum “on” duration for host interface, when in pulse mode. 0: 100µs (use only if ODR < 4kHz) 1: 8µs (required if ODR ≥ 4kHz, optional for ODR < 4kHz) Other Settings: Reserved

21.54 INT_PULSE_MIN_OFF_INTF0

Name: INT_PULSE_MIN_OFF_INTF0
Address: 107 (6Bh)
Serial IF: R/W
Reset value: 0x01
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	INT0_TDEASSERT_DISABLE	INT0 interrupt pulse minimum “off” duration for host interface, indicates minimum interrupt de-assertion duration. 0: 100µs 1: 8µs Other Settings: Reserved

21.55 INT_PULSE_MIN_OFF_INTF1

Name: INT_PULSE_MIN_OFF_INTF1
Address: 108 (6Ch)
Serial IF: R/W
Reset value: 0x01
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:3	-	Reserved
2:0	INT1_TDEASSERT_DISABLE	INT1 interrupt pulse minimum “off” duration for host interface, indicates minimum interrupt de-assertion duration. 0: 100µs 1: 8µs Other Settings: Reserved

21.56 ISR_0_7

Name: ISR_0_7
Address: 110 (6Eh)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_STATUS_ON_DEMAND_PIN_0	For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred.
4	-	Reserved
3	INT_STATUS_EXT_ODR_DRDY_PIN_0	For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.

2:1	-	Reserved
0	INT_STATUS_ACCEL_DRDY_PIN_0	For IRQ0 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.

21.57 ISR_8_15

Name: ISR_8_15
Address: 111 (6Fh)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_STATUS_ON_DEMAND_PIN_1	For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred.
4	-	Reserved
3	INT_STATUS_EXT_ODR_DRDY_PIN_1	For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.
2:1	-	Reserved
0	INT_STATUS_ACCEL_DRDY_PIN_1	For IRQ1 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.

21.58 ISR_16_23

Name: ISR_16_23
Address: 112 (70h)
Serial IF: R/C
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_STATUS_ON_DEMAND_PIN_2	For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of on demand event. 0: Interrupt did not occur. 1: Interrupt occurred.
4	-	Reserved
3	INT_STATUS_EXT_ODR_DRDY_PIN_2	For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of EXT ODR DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.
2:1	-	Reserved
0	INT_STATUS_ACCEL_DRDY_PIN_2	For IRQ2 interface, if this interrupt status bit is enabled, this bit is to flag the occurrence of Accel DRDY event. 0: Interrupt did not occur. 1: Interrupt occurred.

21.59 STATUS_MASK_PIN_0_7

Name: STATUS_MASK_PIN_0_7
Address: 113 (71h)
Serial IF: R/W
Reset value: 0x3F
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_ON_DEMAND_PIN_0_DIS	For IRQ0, on-demand DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ON_DEMAND_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.
4	-	Reserved
3	INT_EXT_ODR_DRDY_PIN_0_DIS	For IRQ0, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.
2:1	-	Reserved
0	INT_ACCEL_DRDY_PIN_0_DIS	For IRQ0, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_0 status bit is 1. 0: Enable the Interrupt pin assertion.

		1: No Interrupt pin assertion.

21.60 STATUS_MASK_PIN_8_15

Name: STATUS_MASK_PIN_8_15
Address: 114 (72h)
Serial IF: R/W
Reset value: 0x3F
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_ON_DEMAND_PIN_1_DIS	For IRQ1, on-demand DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ON_DEMAND_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.
4	-	Reserved
3	INT_EXT_ODR_DRDY_PIN_1_DIS	For IRQ1, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.
2:1	-	Reserved
0	INT_ACCEL_DRDY_PIN_1_DIS	For IRQ1, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_1 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.

21.61 STATUS_MASK_PIN_16_23

Name: STATUS_MASK_PIN_16_23
Address: 115 (73h)
Serial IF: R/W
Reset value: 0x3F
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	INT_ON_DEMAND_PIN_2_DIS	Enables the eDMP to be run once when IRQ2 is triggered by setting the EDMP_ON_DEMAND_EN bit.
4	-	Reserved
3	INT_EXT_ODR_DRDY_PIN_2_DIS	For IRQ2, ODR DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_EXT_ODR_DRDY_PIN_2 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.
2:1	-	Reserved
0	INT_ACCEL_DRDY_PIN_2_DIS	For IRQ2, accel DRDY event, this is to enable the interrupt pin assertion when the INT_STATUS_ACCEL_DRDY_PIN_2 status bit is 1. 0: Enable the Interrupt pin assertion. 1: No Interrupt pin assertion.

21.62 INT_I2CM_SOURCE

Name: INT_I2CM_SOURCE
Address: 116 (74h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	INT_STATUS_I2CM_SMC_EXT_ODR_EN	0: Does not automatically trigger eDMP operation on target ODR 1: Automatically triggers eDMP operation on target ODR
0	-	Reserved

21.63 ACCEL_WOM_X_THR

Name: ACCEL_WOM_X_THR
Address: 126 (7Eh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	WOM_X_TH	Set X-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg)

21.64 ACCEL_WOM_Y_THR

Name: ACCEL_WOM_Y_THR
Address: 127 (7Fh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	WOM_Y_TH	Set Y-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg)

21.65 ACCEL_WOM_Z_THR

Name: ACCEL_WOM_Z_THR
Address: 128 (80h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	WOM_Z_TH	Set Z-axis Wake on Motion threshold Wake on Motion thresholds are expressed in fixed “mg” independently of the selected full-scale (format <U,8,0>, range [0g : 1g], resolution 1g/256=~4mg)

21.66 SELFTEST

Name: SELFTEST
Address: 144 (90h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	EN_GZ_ST	0: Z-axis gyroscope self-test is not enabled 1: Z-axis gyroscope self-test is enabled Can be changed on-the-fly.
4	EN_GY_ST	0: Y-axis gyroscope self-test is not enabled 1: Y-axis gyroscope self-test is enabled Can be changed on-the-fly.
3	EN_GX_ST	0: X-axis gyroscope self-test is not enabled 1: X-axis gyroscope self-test is enabled Can be changed on-the-fly.
2	EN_AZ_ST	0: Z-axis accelerometer self-test is not enabled 1: Z-axis accelerometer self-test is enabled Can be changed on-the-fly.
1	EN_AY_ST	0: Y-axis accelerometer self-test is not enabled 1: Y-axis accelerometer self-test is enabled Can be changed on-the-fly.
0	EN_AX_ST	0: X-axis accelerometer self-test is not enabled 1: X-axis accelerometer self-test is enabled Can be changed on-the-fly.

21.67 IPREG_MISC

Name: IPREG_MISC
Address: 151 (97h)
Serial IF: R
Reset value: 0x02
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1	EDMP_IDLE	0: Indicates eDMP is busy. 1: Indicates eDMP is idle.
0	-	Reserved

21.68 SW_PLL1_TRIM

Name: SW_PLL1_TRIM
Address: 162 (A2h)
Serial IF: R
Reset value: Defined on a pre-device basis
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	SW_PLL1_TRIM	Stores variation of PLL frequency test measurement vs. target value, used for SW applications. Value to trim =(PLL_measurement – 6144000Hz) / 6144000Hz * 2540. 6144000Hz is the target PLL freq. 2540 is the resolution coefficient: max register range / max oscillator frequency error = (2^7 - 1) / 5%, with a sign bit.

21.69 FIFO_SRAM_SLEEP

Name: FIFO_SRAM_SLEEP
Address: 167 (A7h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1:0	FIFO_GSLEEP_SHARED_SRAM	Set selected SRAM bank global sleep mode **Bit 0:** 1. When set to 1: SRAM bank-0 will remain enabled 2. When 0: permits SRAM bank-0 to go to sleep mode a. SRAM bank goes to sleep, if not allocated as FIFO memory space b. If allocated as FIFO memory space, remains active unless FIFO is empty and sensors are off **Bit 1:** 1. When set to 1: SRAM bank-1 will remain enabled 2. When 0: Permits SRAM bank-1 to go to sleep mode a. SRAM bank goes to sleep, if not allocated as FIFO memory space b. If allocated as FIFO memory space, remains active unless FIFO is empty and sensors are off

22 USER BANK IPREG_SYS1 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS1. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

22.1 IPREG_SYS1_REG_42

Name: IPREG_SYS1_REG_42
Address: 42 (2Ah)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_X_OFFUSER[7:0]	Low bits for X-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.2 IPREG_SYS1_REG_43

Name: IPREG_SYS1_REG_43
Address: 43 (2Bh)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_X_OFFUSER[13:8]	Upper bits for X-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.3 IPREG_SYS1_REG_56

Name: IPREG_SYS1_REG_56
Address: 56 (38h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Y_OFFUSER[7:0]	Low bits for Y-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.4 IPREG_SYS1_REG_57

Name: IPREG_SYS1_REG_57
Address: 57 (39h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_Y_OFFUSER[13:8]	Upper bits for Y-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.5 IPREG_SYS1_REG_70

Name: IPREG_SYS1_REG_70
Address: 70 (46h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	GYRO_Z_OFFUSER[7:0]	Low bits for Z-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.6 IPREG_SYS1_REG_71

Name: IPREG_SYS1_REG_71
Address: 71 (47h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	GYRO_Z_OFFUSER[13:8]	Upper bits for Z-gyro offset programmed by user. Range is ±62.5dps, resolution is 7.5mdps.

22.7 IPREG_SYS1_REG_166

Name: IPREG_SYS1_REG_166
Address: 166 (A6h)
Serial IF: R/W
Reset value: 0x1B
Clock Domain: MCLK

BIT	NAME	FUNCTION
7	-	Reserved
6:5	GYRO_SRC_CTRL	Gyro SRC CTRL: 0: Interpolator and FIR filter off 1: Interpolator off and FIR filter on 2: Interpolator on and FIR filter on 3: Reserved (debug mode)
4:0	-	Reserved

22.8 IPREG_SYS1_REG_170

Name: IPREG_SYS1_REG_170
Address: 170 (AAh)
Serial IF: R/W
Reset value: 0x0A
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:5	-	Reserved
4:1	GYRO_LP_AVG_SEL	Gyro Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved
0	-	Reserved

22.9 IPREG_SYS1_REG_172

Name: IPREG_SYS1_REG_172
Address: 172 (ACh)
Serial IF: R/W
Reset value: 0x80
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:5	-	Reserved
4	GYRO_LPF_BYP	0: LPF in Gyro UI signal path not bypassed for all axes. 1: LPF in Gyro UI signal path bypassed for all axes.
3	-	Reserved
2:0	GYRO_UI_LPFBW_SEL	Selects cut-off bandwidth for Gyro UI path LPF 000: Bypass 001: ODR/4 010: ODR/8 011: ODR/16 100: ODR/32 101: ODR/64 110: ODR/128 111: ODR/128

Note: When the FIR AAF is enabled, the signal path BW is decided by the FIR AAF and UI LPF combination. Please refer to AN-000365 ICM-456xx User Guide for details.

23 USER BANK IPREG_SYS2 REGISTER MAP – DESCRIPTIONS

This section describes the function and contents of each register within user bank IPREG_SYS2. The registers described in this section are indirect access registers. Section 13 describes the procedure for accessing indirect access registers.

23.1 IPREG_SYS2_REG_24

Name: IPREG_SYS2_REG_24
Address: 24 (18h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_X_OFFUSER[7:0]	Low bits for X-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.2 IPREG_SYS2_REG_25

Name: IPREG_SYS2_REG_25
Address: 25 (19h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	ACCEL_X_OFFUSER[13:8]	Upper bits for X-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.3 IPREG_SYS2_REG_32

Name: IPREG_SYS2_REG_32
Address: 32 (20h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Y_OFFUSER[7:0]	Low bits for Y-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.4 IPREG_SYS2_REG_33

Name: IPREG_SYS2_REG_33
Address: 33 (21h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	ACCEL_Y_OFFUSER[13:8]	Upper bits for Y-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.5 IPREG_SYS2_REG_40

Name: IPREG_SYS2_REG_40
Address: 40 (28h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:0	ACCEL_Z_OFFUSER[7:0]	Low bits for Z-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.6 IPREG_SYS2_REG_41

Name: IPREG_SYS2_REG_41
Address: 41 (29h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:0	ACCEL_Z_OFFUSER[13:8]	Upper bits for Z-accel offset programmed by user. Range is ±1g, resolution is 0.125mg.

23.7 IPREG_SYS2_REG_123

Name: IPREG_SYS2_REG_123
Address: 123 (7Bh)
Serial IF: R/W
Reset value: 0x14
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:2	-	Reserved
1:0	ACCEL_SRC_CTRL	Accel SRC CTRL: 0: Interpolator and FIR filter off 1: Interpolator off and FIR filter on 2: Interpolator on and FIR filter on 3: Reserved (debug mode)

23.8 IPREG_SYS2_REG_128

Name: IPREG_SYS2_REG_128
Address: 128 (80h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5:3	TMP_DEC_CFG	Temperature sensor decimation factor – controls the processing ODR of the temperature sensor 000: Bypass 001: 2 010: 4 011: 8 100: 16 101: 32 110: 64 111: 128
2:0	TMP_LPF_CFG	Set Temp Sensor Low Pass Filter BW (LNM) 000: Bypass filter 001: 25% of output data rate 010: 17% of output data rate 011:10% of output data rate 100: 4.5% of output data rate 101: 2.1% of output data rate 110: 1% of output data rate 111: 1% of output data rate

23.9 IPREG_SYS2_REG_129

Name: IPREG_SYS2_REG_129
Address: 129 (81h)
Serial IF: R/W
Reset value: 0x02
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:4	-	Reserved
3:0	ACCEL_LP_AVG_SEL	Accel Low Power Mode Averaging Filter Selection 0000: 1x 0001: 2x 0010: 4x 0011: 5x 0100: 7x 0101: 8x 0110: 10x 0111: 11x 1000: 16x 1001: 18x 1010: 20x 1011: 32x 1100: 64x Others: Reserved

23.10 IPREG_SYS2_REG_131

Name: IPREG_SYS2_REG_131
Address: 131 (83h)
Serial IF: R/W
Reset value: 0x00
Clock Domain: MCLK

BIT	NAME	FUNCTION
7:6	-	Reserved
5	ACCEL_LPF_BYP	0: LPF in Accel UI signal path not bypassed for all axes. 1: LPF in Accel UI signal path bypassed for all axes.
4:3	-	Reserved
2:0	ACCEL_UI_LPFBW_SEL	Selects cut-off bandwidth for Accel UI path LPF 000: Bypass 001: ODR/4 010: ODR/8 011: ODR/16 100: ODR/32 101: ODR/64 110: ODR/128 111: ODR/128

Note: When the FIR AAF is enabled, the signal path BW is decided by the FIR AAF and UI LPF combination. Please refer to AN-000365 ICM-456xx User Guide for details.

24 REFERENCE

Please refer to the following application notes for additional information.

- IMU PCB Design and MEMS Assembly Guidelines (AN-000393)
- Understanding IMU Sensor Offset (AN-000257)
- TDK InvenSense IMU Calibration Application Note (AN-000265)
- ICM-456xx User Guide (AN-000365)

25 REVISION HISTORY

Revision Date	Revision	Description
01/10/2025	1.0	Initial Release
05/07/2026	1.1	Updated register reset values (Sections 16.41, 16.42)

TDK InvenSense